

MIM capacitor fabrication

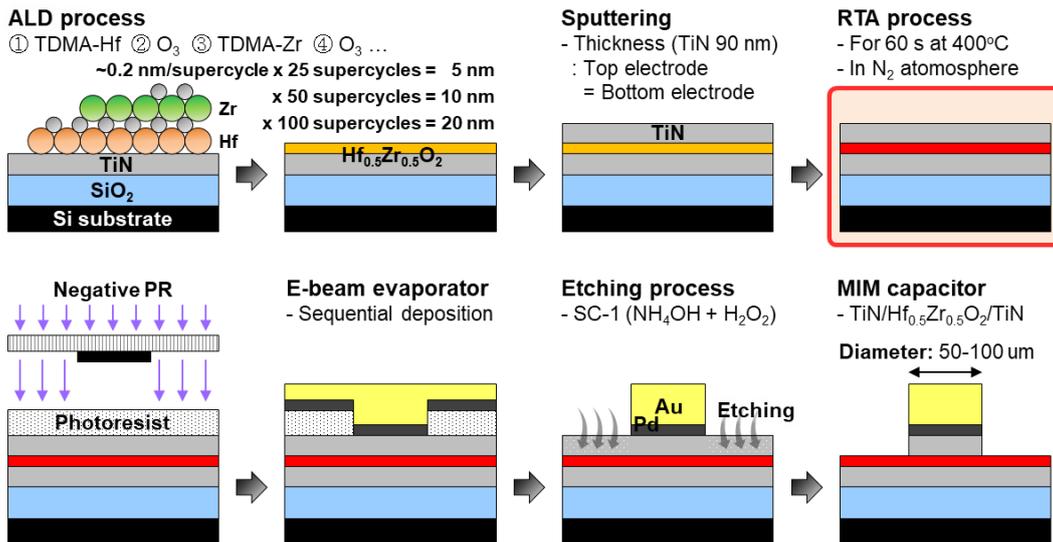


Figure 1. Schematic illustration of the procedure used to fabricate the HZO-based MIM capacitor.

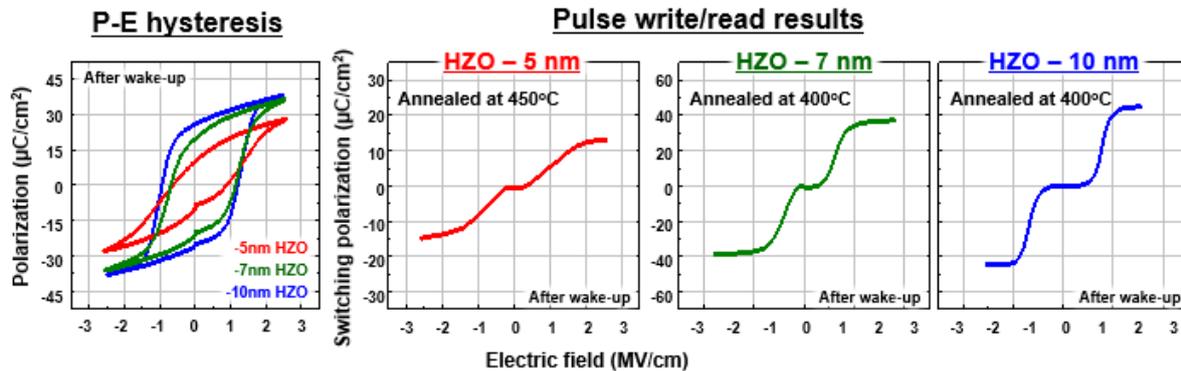


Figure 2. P-E hysteresis and Pulse Read/Write measurements of 5nm HZO (annealed at 450°C), 7nm HZO, 10nm HZO (annealed at 400°C). The pulse read/write measurements replicate actual device operation as an FRAM.

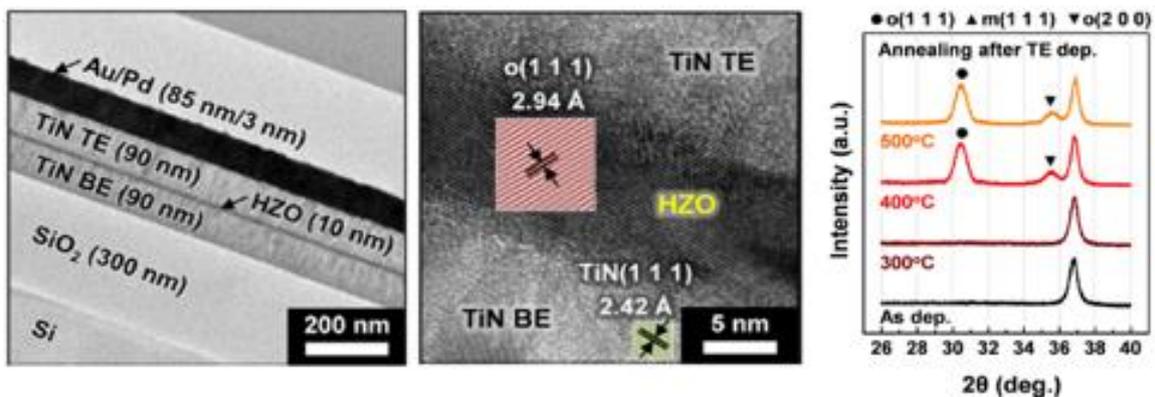


Figure 3. The left images show cross-sectional TEM image of the ferroelectric capacitors fabricated using 10nm HZO, annealed at 400°C. The right image shows GIXRD patterns of 10-nm HZO annealed at various temperatures. The figures show that annealing at 400°C is sufficient for proper crystallization of the ferroelectric orthorhombic phase [3].

(Note: The TEM and GIXRD images from figure 3 are cited from Reference [3] published by our group)