Supplemental File – graphs and charts

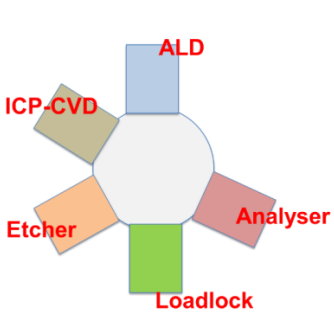

Fig. 1. A cluster tool with ICP etch, ICP CVD and ALD process chambers and surface analysis equipment (SEM, Auger spectrometer and XPS).

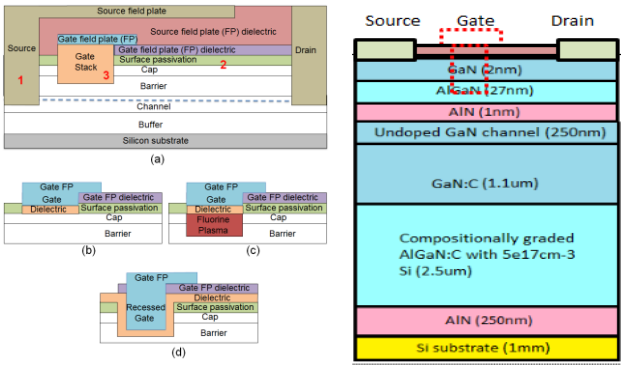

Fig. 2. (Left) Schematic of a generic GaN-on-silicon power transistor; (Right) D-mode device material with a recessed gate prior to dielectric deposition for E-mode device via ALE.

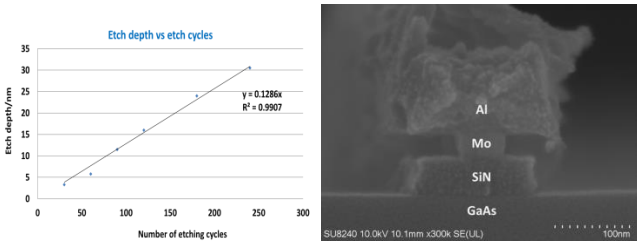

Fig.3. (Left) Relationship between vertical etch depth and number of etching cycles for GaN ALE etch in Cl_2/Ar chemistry; (Right) SEM picture of an ALE lateral etched T-gate metal stack.

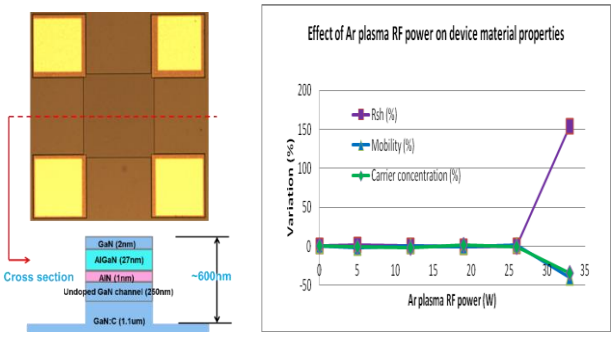

Fig.4. (Left) Van der Pauw device schematic used to evaluate ALE etching damage; (Right) Variation of GaN/AlGaN based device material electric properties at different Ar plasma power in ALE removal step.

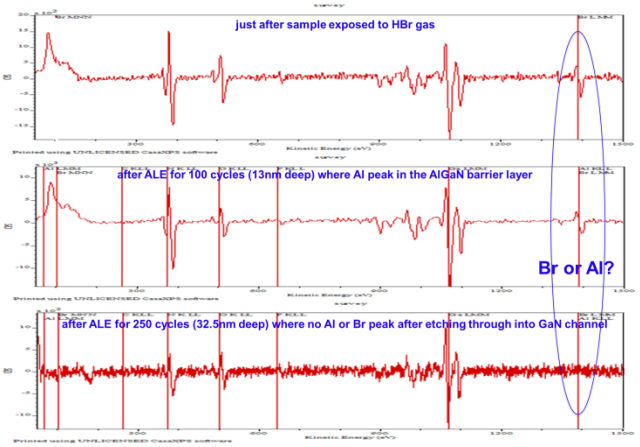

Fig. 5. Typical Auger spectra of the depletion mode GaN-based power device materials, as shown in Fig.2 Right, at different processing steps: before etching on the 1st GaN cap layer (Top); in the AlGaN barrier layer (Middle); in the GaN channel layer after removing GaN cap and AlGaN barrier layers (Bottom).

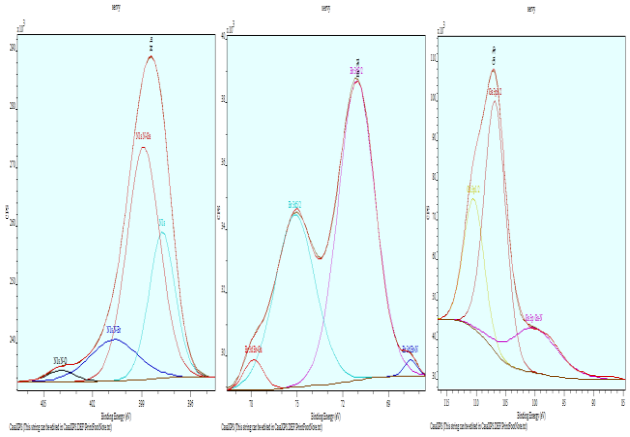

Fig.6. Some typical XPS spectra from the in-situ analysis to show N, Br and Ga presence at the surface after exposing GaN sample to HBr gas flow (where the left one from N 1s, the middle one from Br 3d, and the right one from Ga 3p, respectively).