Live Session
Room Live - Session LI1-MoM
Plenary & ALD Innovator Award Session: Monday Live

Moderators: Christophe Detavernier, Ghent University, Belgium, Erwin Kessels, Eindhoven University of Technology, the Netherlands

10:00am **LI1-MoM-7 Plenary & ALD Innovator Award Session Welcome Introduction***, **Christophe Detavernier**, J Dendooven,* Ghent University, Belgium*; P Poodt,* TNO/Holst Center, Netherlands*; E Kessels,* Eindhoven University of Technology, Netherlands*; H Knoops,* Oxford Instruments Plasma Technology, Netherlands*; J de Marneffe,* IMEC, Belgium

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10:15am **LI1-MoM-8 Meet the ALD 2020 Innovator Awardee***, **Mikko Ritala**,* University of Helsinki, Finland **INVITED**

Meet the ALD 2020 Innovator Awardee Mikko Ritala of the University of Helsinki, Finland

10:30am **LI1-MoM-9 Selective and Atomic Scale Processes to Enable Future Nano-Electronics***, **Robert Clark**,* TEL Technology Center, America, LLC **INVITED**

The economic driving force of Moore's law has enabled scaling of semiconductor devices to the point that modern feature sizes can be measured in atomic dimensions.[1,2] As shrinking the device footprint becomes increasingly difficult a new scaling paradigm making use of vertical scaling has emerged, initially by adopting non-planar devices, and now by stacking devices on top of one another to create 3D architectures as well.[3] Fabricating 3-dimensional electronic structures with atomic scale dimensions in high yields presents a number of daunting process challenges. Among these are the need to tightly control film thickness, uniformity, morphology, and composition within high aspect ratios. The need for selective deposition of functional films as well as layers used simply for patterning or alignment presents another challenge if we are to transition towards and more bottom-up style of nanomanufacturing. Selective and atomic scale processes are being developed in order to enable a number of self-aligned process schemes as well as scaling boosters required for future device nodes. Dielectric on dielectric (DoD) selective deposition is being developed to enable fully self-aligned vias to address edge placement error challenges encountered when manufacturing advanced interconnects. Selective metal on metal (MoM) depositions are useful for depositing metal capping layers as well as hardmasks. Scaling boosters such as super-vias and buried power rails could benefit from well-controlled processes with topographical selectivity. And dielectric on metal depositions (DoM) could provide relief from the growing overburdens needed to enable chemical mechanical planarization during replacement metal gate integration in the front end. Progress in these areas as well as future needs and an outlook on future device scaling pathways will be presented.

1. (a) Moore, G. E., *Electronics* **1965,***38* (8); (b) Bohr, M.,*Technical Digest of the IEEE International Electron Devices Meeting*, Washington, D.C., **2011**; pp 1-6.

2. Clark, R.D., *Materials* **2014,***7* (4), 2913-2944.

3. Clark, R., Tapily, K., Yu, K.-H., Hakamata, T., Consiglio, S., O'Meara, D., Wajda, C., Smith, J., Leusink, G. *APL Materials***2018**, 6, 050283.

11:00am **LI1-MoM-11 The First Application of ALD Technology in Display Industry***, **Hyun-Chul Choi**,* LG Display, Republic of Korea **INVITED**

TFT-LCD, which has dominated the display industry for the past 20 years, is gradually being replaced by OLED in recent years. OLED is superior to TFT-LCD in terms of image quality and design, but requires more advanced technologies and processes. OLED is vulnerable to moisture and oxygen due to the nature of organic materials, so encapsulation of OLED device plays a very important role to ensure the reliability of OLED. In small-size OLED products, thin film encapsulation (TFE) technology is used to form inorganic and organic layers on OLED device to protect OLED from moisture and oxygen. Atomic layer deposition, one of the semiconductor technologies, is successfully used to form high-quality TFE, which greatly improved the reliability of OLED. In addition, in order to enhance the performance of oxide-based large-size OLED products, MOCVD technology is steadily being researched and developed.

This plenary speech introduces the contribution of semiconductor technologies to the performance and quality of OLED. In addition, we will discuss the possibility of what semiconductor technologies can be applied for the future development of OLED technology.

11:30am **LI1-MoM-13 ALD on Powders for Catalysis***, **Frank Rosowski**,* BASF SE, Germany **INVITED**

Atomic Layer Deposition (ALD) is mainly applied in microelectronics as a thin film deposition technique. In academic research, ALD is also applied for synthesis of catalysts. The main challenge for ALD in this research field is the morphology of the substrate materials, usually small particles with high specific surface areas, e.g. up to 1000 m2/g for zeolites. In industry, catalytic reactors can hold packed beds of several tons of catalyst mass, exposing huge surface areas. But even in academia, where typical reactor loadings are on the gram scale, the surface areas to coat are in the range of hundreds of square meters, several orders of magnitude higher than for any wafer in the semiconductor industry.

At BasCat, the UniCat – BASF JointLab at Technische Universität Berlin, several projects use ALD as tool to synthesize and modify catalysts. In the field of supported metal catalysts, research is so far done along well-established lines of work, e.g. modifying supported metal catalysts with metal oxide layers, e.g. ZnO, alumina, and alucone. But the research focus lies on catalysts used for selective oxidation reactions, typically consisting of mixed metal oxides or phosphates. Catalysts are usually prepared in two batch sizes. For establishing suitable ALD process conditions, a sample size of about 1.0 cm3 is used. In a second step, catalyst amounts of 10 – 25 cm3 are prepared. It is important that process conditions established on the small scale are easily transferrable to the large scale.

For this purpose, a new and unique test facility was installed at BasCat equipped with a thermogravimetric balance as analytical small scale ALD reactor and a second reactor for catalyst synthesis on a large scale via ALD.[1] Based on our first ALD results, a fixed bed was chosen as reactor geometry for the analytical reactor and the synthesis reactor.

It was demonstrated that the fixed bed geometry is suitable for ALD yielding homogeneously covered substrates, and that scaling-up from 1.0 cm3 to 10 cm3 is possible.[2]

The combination of analytical reactor and synthesis reactor was then successfully used for modifying supported metal catalysts with layers of alumina and alucone,[3] and zinc oxide.[4] Other works included the deposition of rhenium on silver and phosphorus on vanadia.[5]

[1] Strempel, V. E., Naumann d'Alnoncourt, R., Driess, M. and Rosowski, F., Rev. Sci. Instrum., 074102. 2017

[2] Strempel, V., Knemeyer, K., Naumann d'Alnoncourt, R., Driess, M. and Rosowski, F.,Nanomaterials, 365. 2018

[3] Ingale, P., Guan, C., Kraehnert, R., Naumann d´Alnoncourt, R., Thomas, A., and Rosowski, F., Catalysis Today, submitted

12:00pm **LI1-MoM-15 The Flip Side of the Story: Atomic Layer Etching***, **Keren Kanarik**,* Lam Research Corp. **INVITED**

For the past 30 years, this conference has been largely dedicated to understanding the addition of atomically thin films. The flip side of that story is the removal of thin layers of material – Atomic Layer Etching – which only this past decade moved from "lab to fab" and into the mainstream. What took so long? What assumptions had to be revisited? In retrospect, we now understand why silicon was not the best case study system after all. More amenable materials have made it easier to find important benefits, such as the smoothing effect. A new operating regime led us to rethink the definition of an energy window. Such insights are proving vitally important for improving productivity and thus expanding the number of beneficial applications of this technology. While deposition has certainly led the way, etching offers a perspective from the flip side to understanding processes at the atomic scale. This plenary talk will share insights from the past decade, in hopes of continuing to push these complementary techniques forward in building the next generation of semiconductor devices.

12:30pm **LI1-MoM-17 JVST Best Paper Award, Closing Remarks, & Sponsor Thank You***, C Detavernier, J Dendooven,* Ghent University, Belgium*; P Poodt,* TNO/Holst Center, Netherlands*; **Erwin Kessels**,* Eindhoven University of Technology, Netherlands*; H Knoops,* Oxford Instruments Plasma Technology, Netherlands*; J de Marneffe,* IMEC, Belgium

JVST Best Paper Award will be presented. You are now welcome to view all ALD/ALE On Demand Presentations

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