ALD Applications
Room Van Rysselberghe - Session AA2-TuM2

ALD for FEOL

Moderators: Cheol Seong Hwang, Seoul National University, Jonas Sundqvist, BALD Engineering AB

10:45am **AA2-TuM2-1 High ALD Equipment and Precursor Demand and 5-Year Forecast Due to Continued Semiconductor Device Scaling and Fab Expansions**, ***Jonas Sundqvist,*** Stockholm, Sweden **INVITED**

The global market for ALD and CVD are experiencing high growth [1]. Total precursor market grew 20% in 2021to approach US$1.4B and will increase by 13% topping US$1.5B in 2022

1. Metal & High-k CAGR (2021 to 2026) = 9.3%
2. Dielectric CAGR (2021 to 2026 = 6.9%

The growth is driven by advanced logic, DRAM and 3DNAND memory chip fabrication needs. In the short-term forecast, sees the global semiconductor market as very healthy with 15-20% YoY growth in 2021 revenues [2], and overall critical materials market growth >7% YoY. All ALD/CVD metal precursors are in healthy demand, since ALD is critical for fabs running 22-45nm nodes as well as for fabs at the leading edge at 16/14 nm and below. In particular, Co and Hf precursors saw high growth in 2020 and 2021 and are forecasted to see strong demand through 2026. Zr used for DRAM capacitors saw a lower growth but is a big segment on its ow. Ru metal is slowly replacing some of the Co and W interconnects on the most advanced logic chips, with anticipated precursor revenue growth to US$10M in 2025 for this highly strategic material. Metals to observe the next years include Mo, Nb and La. Implementation of ALD in emerging new technologies has high potential since all industries are at Giga scale in HVM: PV, Display, MEMS, Power Electronics, LED/µLED, Optical, Lithium Battery, Solid State Fuel Cells, Parts and powder coating and Medical.

ALD materials and OEM tools are needed for multi-patterning lithography used with DUV Immersion and with EUV in leading logic and memory fabs. Multi-patterning typically uses low-temperature PEALD, either in clusters of 8-16 single-wafer chambers, or in “Spatial” high-throughput tools. It is anticipated that fab investments in Asia will allow South Korean and Chinese OEMs to win near-term ALD orders, and they may soon compete with US, EU, and Japanese OEMs in the global tool market for standard processes that are commoditized. Recent actions taken by the new US administration has boosted logic fab investments in the US and several leading-edge fab investments are on the horizon the next three to five years, which will generate a need for both ALD equipment and a healthy precursor supply chain on all materials above going forward.

[1] TECHCET LLC CA, Critical Materials Reports™ 2021

[2] TECHCET LLC CA, 2021 Critical Materials Council (CMC) Conference, Apr. 14-15, San Diego, USA

11:15am **AA2-TuM2-3 High-k Gate Dielectrics for ScAlN Barrier HEMT Structures**, ***Neeraj Nepal,*** *V. Wheeler,* U.S. Naval Research Laboratory*; . Downey,* U.S. Army Research Laboratory*; . Hardy, D. Meyer,* U.S. Naval Research Laboratory

There has been increased interest in ScAlN-barrier high electron mobility transistors (HEMTs) as ScAlN has larger spontaneous and piezoelectric polarization fields than those in GaN and AlN, which can lead to larger two dimensional electron gas (2DEG) densities. Also, ScAlN with 18% Sc content is nearly latticed matched with GaN and has bandgap of 5.65 eV. Thus, ScAlN can provide a strain-free barrier for GaN HEMT structures with high carrier concentration. Recently, we have demonstrated ScAlN-barrier GaN HEMT structures with electron mobility of 910 cm^2/V-s and 2DEG density >$3x10^{13}$ cm^{-2} [1]. However, these ScAlN/GaN HEMT devices still suffer from high leakage current [2]. Integrating gate dielectrics into these novel ScAlN-barrier HEMTs is necessary to decrease the leakage current, maintain high electric field breakdown and mitigate dc-RF dispersion in order to realize the full potential of these devices.

In this talk we report growth optimization and electrical properties of atomic layer deposition (ALD) grown TiO_2 gate dielectric on ScAlN-barrier HEMTs using Ultratech Fiji Gen2 ALD reactor. ALD process windows were initially monitored and optimized on Si substrates using *in-situ* ellipsometry. Films were deposited using tetrakis(dimethylamino)titanium (TDMAT) and an Ar/O_2 plasma at 300W. The TDMAT precursor temperature was maintained at 75 °C, while the pulse duration was varied from 0.25 to 0.35 sec. The plasma gas chemistry was also optimized. Optimal deposition parameters were used as initial condition to further optimize ALD conditions on ScAlN surface. On ScAlN barrier HEMT structures, deposition temperature was varied from 150 to 350 °C.

Atomic force microscopy was measured before and after ALD deposition showing minimal change in roughness as a result of the TiO_2 deposition.Contactless resistivity measurements performed before and after ALD and were also consistent, indicating that no plasma induced damage was occurring during ALD gate deposition. Vertical current-voltage and capacitance-voltage measurements were made on a Schottky-contacted HEMT structure and compared to devices with TiO_2 gate dielectrics deposited at different temperatures to discern the full electrical impact. As an example, an extracted dielectric constant of TiO_2 layer deposited at 200°C with O_2 flow of 20 sccm was 50 with no significant change in 2DEG density (changed from $2.7x10^{13}$ cm^{-2} to $2.6x10^{13}$ cm^{-2}after TiO_2 layer). Finally, we will present the band alignment of an optimum ALD TiO_2 on ScAlN structure using x-ray photoelectron spectroscopy.

References:

1. Hardy et al., *Appl. Phys. Lett.***110**, 162104 (2017).
2. Green *et al*., *IEEE Electron Device Letters***40**, 1056 (2019).

11:30am **AA2-TuM2-4 Ultra-thin High-κ Dielectrics Growth by ALD on MoS_2**, ***Emanuela Schilirò,*** *R. Lo Nigro,* CNR-IMM, Italy*; S. Panasci,* CNR-IMM, Department of Physics-University of Catania, Italy*; A. Mio,* CNR-IMM, Italy*; S. Agnello, F. Gelardi,* Department of Physics and Chemistry, University of Palermo, Italy*; F. Roccaforte, F. Giannazzo,* CNR-IMM, Italy

MoS_2 is one of the most investigated 2D-materials belonging to the wide class of transition metal dichalcogenides (TMDs). The great interest in MoS_2 is mainly attributable to the existence of a bandgap that, differently from graphene, makes it suitable also for logic and switching devices. In particular, monolayer-MoS_2 presents a direct-gap semiconducting behavior with a bandgap of 1.8 eV. However, to guarantee high-performance in terms of field-effect mobility (100-500 cm^2/V s), sub-threshold swing (~ 70 mV/dec) and on/off ratio (~ 10^8) the MoS_2-devices requires high-κ dielectrics (Al_2O_3, HfO_2) as top-gate layers. Atomic layer deposition (ALD) is the most appropriate technique to grow uniform high-κ layers with accurate control of thickness. Nevertheless, the uniformity of ALD-nucleation on 2D surfaces can be poor due to lacking out-of-plane bonds, which should act as nucleation sites. Seed-layers and/or pre-functionalization are, hence, necessary to activate ALD-growth on 2D-materials. Their undesired effects on the interfacial quality with 2D-materials encourage the research of new solutions. The substrate, as the driving force of nucleation, is one of the more promising. In fact, similarly to graphene [1,2], also for MoS_2 [3], a metal substrate (gold), has been demonstrated to be a key factor to obtain uniform ultra-thin layers of Al_2O_3. In this work, a large area of monolayer-MoS_2 was exfoliated from bulk molybdenite to a gold substrate. Direct ALD processes of Al_2O_3 and HfO_2 were carried-out on MoS_2/Au substrate, and the structural and insulating properties of high-k were investigated. In particular, ALD coverage degree was evaluated, using standard and conductive-AFM, since the early stage of nucleation. Lower coverage was found for HfO_2, during the early cycles of deposition (40 cycles), than Al_2O_3. However, for longer processes (80 cycles), both high-k show similar ad optimal coverage (higher 95%) but also propitious structural and insulating properties already from very ultra-thin thickness (~ 3.5 nm). Uniform, adherent and compact layers were observed by HR-TEM characterization. Homogeneous insulating behavior and congruent breakdown electric field values were demonstrated, for both high-k, by conductive-AFM measurements.

These results can have an important impact on the realization of devices based on large-area MoS_2 membranes.

This work has been supported by the FLAG-ERA JTC2019 project “ETMOS”

[1] B. Dlubak et al Appl. Phys. Lett., 100, p. 173113 (2012).

[2] E. Schilirò et al Adv. Mater. Interfaces 1900097 (2019).

[3] E. Schilirò et al Adv. Mater. Interfaces., 2101117 (2021).

11:45am **AA2-TuM2-5 Fabrication of a MOSFET Based on ZnO Using an Atomic Layer 3D-printer***, **Sonja Stefanovic**, N. Gheshlaghi,* Friedrich-Alexander-University Erlangen-Nürnberg (FAU), Germany*; I. Kundrata,* Friedrich-Alexander-University Erlangen-Nürnberg (FAU), Dominica*; D. Zanders,* Ruhr Universität Bochum, Germany*; J. Bachmann,* Friedrich-Alexander-University Erlangen-Nürnberg (FAU), Germany

Area-selective atomic layer deposition (as-ALD) is bottom-up nanofabrication by using atoms as building blocks. As-ALD has the potential to overcome many of the challenges the semiconductor industry is facing by enabling self-aligned fabrication, instead of lithography's cost, complexity. However, the main challenges in as-ALD are the need for pre-patterned substrates, defects outside of the desired growing area resulting from insufficient selectivity, and a limited selection of substrate materials that allow deposition.

We have devised and manufactured a direct patterning atomic layer 3D-printer (AL 3D-printer) equipment with a special nozzle design that enables producing direct patterning of various materials with atomic precision. Our invented device is a flexible and efficient tool for reducing the cost and time spent for designing and manufacturing. AL 3D-printer in principle functions similar to conventional g-ALD and all the commercially available precursors which have been used in g-ALD are compatible with our invented equipment. i.e. we have already deposited different materials such as TiO_2, Pt, SiO_2, Al_2O_3 successfully. In addition, the special design of the device allows us to explore new reactions with precursors which are not preferred because of their low vapour pressure or less reactivity.

In this work, we focused on the development of ZnO films with water and a new precursor named $Zn(DMP)_2$(DMP = dimethylaminopropyl) which has a very low vapour pressure compared to a well-studied diethylzinc ($ZnEt_2$) precursor which has a very high vapour pressure and reactivity. Using the proposed direct patterning technique, high-aspect-ratio patterns of ZnO films with our new precursor were fabricated. The patterned films are closed-packed with sharp edges and residual-free surfaces. Our characterization results on the deposited ZnO films with our new precursor shows they have the same structure and composition as with $ZnEt_2$. The produced films are crystalline and the crystals are oriented in a roughly isotropic manner. The growth rate is 1.0 Å per cycle at 200°C. Finally, to assess the reliability and feasibility of the proposed direct patterning method in microelectronic applications, we fabricate a metal oxide transistor MOSFET to demonstrate the practical applications of the device.

Author Index

Bold page numbers indicate presenter