Wednesday Morning, June 29, 2022

Plenary Session
Room Auditorium - Session PS-WeM1

Plenary Session III

Moderators: Jolien Dendooven, Ghent University, Belgium, Christophe Detavernier, Ghent University, Belgium, Paul Poodt, Holst Centre / TNO

8:45am **PS-WeM1-2 ALD 2022 Innovator Awardee Talk: Prospects of Atomic Layer Deposition for Cell-Stacking Technology of Semiconductor Memory Devices**, ***Cheol Seong Hwang,*** Seoul National University, Korea (Republic of) **INVITED**

Atomic layer deposition (ALD) contributed to the scaling down of semiconductor devices for both memory and foundry sectors through its unmatched excellence in controlling the thickness and performance over three-dimensional structures. Furthermore, the types of materials that can be grown by the ALD have expanded from simple binary oxides to diverse and multi-component during the past decades, enabling further exploitation of ALD toward futuristic semiconductor devices. However, one of the biggest challenges in the general semiconductor business is the extremely high cost of fabrication, which is mainly related to the lithography processes requiring extreme-UV scanners. This problem is more severe for the memory business because of the relatively low chip prices than the processors. The memory industry was already aware of this problem, and the NAND flash had evolved from the planar- to the cell-stacked structure when the design rule reached ~ 14 nm. A similar trend may come when dynamic random access memory (DRAM) reaches the ~ 10 nm technology node. It is still unclear when the DRAM industry will hit the ~ 10 nm technology node, but it will come within ~ 10 years. Looking back to the history of cell-stacking technology development of the NAND flash, which took ~ 6-7 years from the first paper publication to the first customer sample fabrication, it is time to focus more on the stackable DRAM cell technology. Besides, the currently suggested cell-stack structure of DRAM indicates several opportunities and challenges for the nano-scale thin film growth area via ALD; it may require an even higher performance of the material, ca. ultrahigh-*k* capacitor dielectrics. Nonetheless, it also offers a chance to use slightly thicker thin films in those structures that are not useful for the planar structures due to the stringent lateral geometry limitations.

This talk will shortly review the status and challenges of the current DRAM and NAND devices, especially from the viewpoints of ALD films. Then, it will cover the suggested or expected memory cell structures based on the cell-stacking technology, in which the NAND is more apparent and DRAM is more obscure. Then, the requirements and challenges for the ALD films for those structures and processing are reviewed. Some of the recent progress achieved in the author's group will be described. The talk will end with remarks on the prospect of memory and the related ALD industry.

9:15am **PS-WeM1-4 ALD Student Award Finalist Talk: Improving Self-Aligned Atomic Layer Deposited Gate Stacks for Electronic Applications**, ***Amy Brummer,*** *D. Aziz, M. Filler, E. Vogel,* Georgia Institute of Technology

Area-selective atomic layer deposition (AS-ALD) is a promising method for the formation of bottom-up structures that can be inherently aligned with the underlying substrate material which would benefit electronics fabrication by reducing the number of photolithography steps and eliminating overlap capacitance. In this work, a previously developed process of forming a self-aligned gate stack [1] is used with various Si oxidation techniques to study methods to improve the semiconductor-oxide interface quality and reduce defect density. A planar adaptation of the SCALES process [2] is combined with AS-ALD to form a self-aligned gate stack based on the underlying Si doping profile. First, a poly(methyl methacrylate) (PMMA) brush is grown from a planar Si surface patterned with regions of light and heavy doping. The PMMA brush is then selectively etched with KOH, which etches lightly doped Si much faster than heavily doped Si, resulting in a patterned PMMA film that covers heavily doped Si with exposed lightly doped Si regions. The patterned PMMA film enables the selective deposition of HfO_2 and Pt on the lightly doped regions via AS-ALD by deactivating the heavily doped Si regions. XPS data confirms selective deposition of HfO_2 and Pt (Figure 1), ultimately forming a metal-oxide-semiconductor (MOS) structure suitable for a MOSFET gate stack. And electrical characterization shows expected C-V behavior for a Pt-HfO_2-Si MOS capacitor structure (Figure 2). To improve electrical performance and reduce defect density, the impact of wet oxidation techniques (e.g. H_2O_2, SC-1 clean, SC-2 clean) prior to HfO_2 ALD on the semiconductor-oxide interface is examined. The MOS capacitor structures are characterized with ellipsometry, XPS and electrical characterization.

This work was supported by DARPA (W911NF2110298), the DOD through the National Defense Science and Engineering Graduate Fellowship Program, and the National Science Foundation (No. CMMI-1916953). This work was performed in part at the Georgia Tech Institute for Electronics and Nanotechnology, a member of the National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation (No. ECCS-2025462).

[1] Brummer, Amy C., et al. *Applied Physics Letters* 119.14 (2021): 142901.

[2] Mohabir, Amar T., et al. *ACS nano* 14.1 (2020): 282-288.

9:30am **PS-WeM1-5 ALD Student Award Finalist Talk: Towards High Throughput Molecular Layer Deposition of Alucone Films**, ***Hardik Jain,*** Holst Centre / TNO, Netherlands*; M. Creatore,* Eindhoven University of Technology, The Netherlands*; P. Poodt,* Holst Centre / TNO, Netherlands

The deposition rate and properties of MLD films are for a large part determined by what happens during the precursor exposure step. In some cases, however, the purge step is of equal importance, for example in the MLD of alucone films using trimethylaluminum (TMA) and ethylene glycol (EG). Due to the porosity of alucone films, the reactants during their exposure step not only react at the film surface but also tend to infiltrate into the film. The subsequent outgassing of the infiltrated reactant can take relatively very long thereby becoming the deposition rate-limiting step. If enough purge time is not provided for the reactant to outgas, it will lead to an additional CVD component alongside MLD in the overall growth. To employ/avoid the CVD component in the deposition process, we have also developed a kinetic model to correlate parameters like exposure times, partial pressures, purge times and deposition temperature to the amount of CVD component in the growth.

Additionally, we also looked into solutions to increase the deposition rate of the alucone films and amongst others found that using a bulkier precursor like DMAI instead of TMA can overcome the problem of precursor infiltration and increase the deposition rate of alucone processes by at least an order of magnitude. In this work, we also present a detailed investigation of MLD of alucone using DMAI as the aluminum precursor. The effect of deposition temperature and reactant purge times on deposition kinetics has been investigated and the DMAI alucone films have been compared with those prepared using TMA for their chemical environment and degradation showing striking similarities between both. The results demonstrate that in some cases less reactive and bulkier precursors like DMAI can indeed be used to increase the deposition rate of an MLD process. We believe that the above work could be extended to other MLD systems and can serve as a guide in designing efficient MLD reactors and processes.

9:45am **PS-WeM1-6 ALD Student Award Finalist Talk: In-situ FTIR Analysis of Selectivity Loss Mechanism of TiO_2 Atomic Layer Deposition on Aminosilane-Passivated SiO_2 and H-terminated Si**, ***Jan-Wilem Clerix,*** KU Leuven, NCSU, Imec, Belgium*; G. Dianat,* NCSU*; A. Delabie,* Imec, KU Leuven, Belgium*; G. Parsons,* NCSU

To increase selectivity in area-selective atomic layer deposition (ALD), research is focused on developing passivation layers that inhibit growth on non-growth surfaces. Such passivation layers have a number of requirements: they should form selectively on the non-growth surface, be stable at the process conditions and be unreactive towards the ALD precursors [1]. Different types of passivation layers have been developed, including self-assembled monolayers, small organic molecules and aminosilanes. The last of those show great promise for implementation in area-selective ALD schemes due to their selective reaction with SiO_2, stability at high temperatures and ability to inhibit both metal and metal oxide ALD.

In this study we further develop the understanding of the mechanisms of inhibition of common ALD precursors such as $TiCl_4$ and H_2O by in-situ Fourier-transform infrared spectroscopy. Firstly, the deposition of N,N-dimethylamino-trimethylsilane (DMATMS) is investigated on OH-terminated SiO_2 (SiO_2-OH) and H-terminated Si (Si-H). DMATMS reacts only with hydroxyl sites (-OH) on the surface, with a preference for isolated -OH. Most reactive sites are consumed in the first seconds of exposure. The fast reaction makes DMATMS ideally suited to be implemented in conventional ALD reactors. When the passivated SiO_2-OH is exposed $TiCl_4$, the formation of Ti-O does not coincide with a loss of trimethylsilyl termination of the surface. Instead, the absorption of $TiCl_4$ is due to unpassivated, H-bonded -OH, which is present since the trimethylsilyl coverage is sterically limited and DMATMS reacts preferentially with isolated -OH. The trimethylsilyl termination is stable against H_2O for extended exposures. On the Si-H, DMATMS serves to passivate any remaining -OH. Any passivation loss can

be linked to loss of H-termination and adsorption of $TiCl_4$ on siloxane bridges. Encouragingly, we see that the addition of DMATMS creates an even better inhibited surface than pristine Si-H.

Overall, we conclude that DMATMS is an excellent choice for passivating agent due to its ability to inhibit a variety of processes and its applicability in passivation-deposition-etch cycles. Nonetheless, passivation of SiO_2-OH could be improved by combination with an additional, smaller passivating agent to limit the impact of steric hindrance.

[1] J. Yarbrough et al., J. Vac. Sci. Technol. A **39**, 021002 (2021).

10:00am **PS-WeM1-7 ALD Student Award Finalist Talk: Sacrificial Etching Kinetics Control Extent of Pattern Alignment in Area-Selective Atomic Layer Deposition (AS-ALD) via Simultaneous Deposition and Etching**, ***Hannah Margavio****, J. Kim,* North Carolina State University*; N. Arellano,* IBM Almaden Research Center*; G. Parsons,* North Carolina State University

By the year 2040, electronic devices are projected to consume ~ 20% of all energy generated on Earth.[1] Therefore, current challenges such as feature misalignment in a semiconductor device, which causes open circuits, excess resistance, and power dissipation and can result in chip failure, must be overcome.[2] Accurate feature alignment from standard lithographic techniques is further hampered by continuous downscaling of integrated circuits, thus bottom-up patterning methods are needed to circumvent inherent variability in lithography. Area-selective atomic layer deposition (AS-ALD) poses a more sustainable patterning alternative to top-down processes by directing precursors to a particular reactive surface chemistry to deposit material only in that region, while preventing growth in an adjacent region.

Our group has previously demonstrated highly selective W-ALD on Si by simultaneously etching a neighboring TiO2 feature with a single precursor set ($SiH_{4(g)}$ and $WF_{6(g)}$) for both reactions.[3] The sacrificial etching reaction maintains selectivity throughout the process by consuming deposition precursors, thereby avoiding unwanted nucleation (Fig. 1). Herein, we show that the extent of selective W growth is controlled by the TiO_2 etching rate. We sequentially dose SiH_4 and WF_6 gases onto 100-nm thick TiO_2 lines patterned on Si (Fig. 2a) and evaluate the extent of selective W growth by scanning electron microscopy (SEM) and energy-dispersive x-ray spectroscopy (STEM-EDS) for various processing temperatures and SiH_4 exposures.

In the initial stages of TiO_2 etching, WF6 diffuses into the bulk of the feature, partially fluorinating it to form a porous oxy-fluoride layer WO_xF_y/TiO_yF_z.[4] We show that at 280 °C (Fig. 2b), the etching rate is too fast, and the oxy-fluoride layer creates a rough sacrificial feature profile from formation of volatile WF_2O_2 and TiF_4. The subsequent SiH_4 dose remains trapped in the low-density layer after purging, initiating parasitic W growth. We show that selectivity can be maintained by controlling the sacrificial feature profile evolution. At lower reaction temperatures, TiO_2 etches slowly and conformally, thus preventing W nucleation.

The presented mechanism for AS-ALD is a way to perform both selective ALD and CVE with the same chemistry and processing conditions. This process not only improves selective W deposition abilities—a valuable material in semiconductor manufacturing—but also shows the success of an integrable ASD process that can be extended to more materials.

[1]Decadal Plan for Semiconductors; SRC, 2021.

[2]Clark, R. et al. APL Mater. 2018

[3]Song, S. K. et al., ACS Nano 2021.

[4]Lemaire, P. C. et al., Chem. Mater. 2017

10:15am **PS-WeM1-8 ALD Student Award Finalist Talk: Depositing Metal Oxides on Metalcones: Enhancing Initial Growth Through O_2 Plasma Densification**, ***Juan Santo Domingo Peñaranda****, M. Minjauw, J. Li, S. Vandenbroucke, J. Dendooven, C. Detavernier,* Ghent University, Belgium

Flexible devices for display/battery applications are gaining traction every day, but moisture sensitivity can be a concern. For this, Thin-Film Encapsulation (TFE) moisture barriers need to be used, but many current technologies rely on rigid barriers that crack and stop performing under flexible stress. As a solution, organic/inorganic thin film stacks are now widely explored for TFE.

In this context, we have studied O_2 plasma densification on MLD alucone[1], titanicone, tincone and zincone. We also investigated the effect of the growth of ALD metal oxides on metalcones with or without prior plasma densification to optimize the deposition of ALD/MLD multilayers.

Upon plasma treatment, all metalcone layers exhibited a similar behaviour. A bilayer structure was evidenced by X-ray reflectivity (XRR), composed of a (~2 nm thick) high-density layer on top of one with metalcone-similar density. The overall film thickness decreased and its evolution in both the dense and less-dense layer could be monitored with in-situ ellipsometry (Figure 1), revealing a saturating behavior. In Fourier-Transform Infrared Spectroscopy (FTIR), plasma-treated metalcones (PT-metalcones) showed a decrease in the C-O region and an increase in the C=O one (Figure 2), similar to aged metalcones. After several months of aging, only an increase in the O-H band was found. X-ray Photoelectron Spectroscopy (XPS) showed a decrease of C content in the top of the layers that did not reach zero. Thus, we conclude that O_2 plasma treatments on metalcones produce a partial densification of the layers. The O_2 radical species oxidise the topmost region of the hybrid film into its corresponding, dense oxide. However, O_2 radicals penetrate deeper down the layer, oxidising the original alcoholic structure into an intermediate ketonic one. According to XPS, a material more similar to an oxycarbide may be formed.

Secondly, metal oxides were grown on top of their respective metalcones, and pristine and PT-metalcones were compared. Using in-situ ellipsometry, growth on pristine metalcones always suffered a delay until the oxide thickness started to increase(Figure 3)[2]. However, an oxide layer immediately started growing on PT-metalcones, from cycle one, offering very accurate oxide thickness control. With this, we hope to have expanded the potential of using stacks of oxides and PT-metalcones for TFE applications. The use of O_2 plasma densifications could hold potential towards film-ratio optimisation for optimum performance at minimal film thicknesses.

1. Santo Domingo Peñaranda et al. *Dalt. Trans.***2021**, *50* (4), 1224–1232
2. Choi et al. *ACS Appl. Mater. Interfaces***2016**, *8* (19), 12263–12271

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