ALD Applications
Room Grand Ballroom H-K - Session AA1-WeM
Memory RRAM, Neuromorphic, NVM

Moderator: Dr. Robert Clark, TEL Technology Center, America, LLC

8:00am **AA1-WeM-1 3D Integrated Device Applications of ALD-Grown Ferroelectric and Oxide-Semiconductor Materials***, **Masaharu Kobayashi**,* University of Tokyo, Japan **INVITED**

Ferroelectric memory is a candidate for lower power memory device. HfO_2-based ferroelectric (FE-HfO_2) has been recently discovered [1], which drives ALD-based ferroelectric (FE) material and opens pathway to high-capacity memory. Oxide semiconductor (OS) such as IGZO is now getting attention for BEOL-compatible transistor channel material [2]. 3D integrated device application requires ALD growth of OS. These two ALD-based materials have been intensively explored in R&D of LSI community as key enablers for energy-efficient computing devices. In this presentation, I will discuss challenge and opportunity of ALD process for 3D integrated device applications based on our recent research progress.

(1) Monolithic 3D integration of OS FET and $HfZrO_2$ FE-capacitor

HfO_2-based FE-capacitor can be formed at BEOL because of its low thermal budget. Monolithic integration of embedded FeRAM can be realized by FE-HfO_2 and OS FET, which enables high density and high bandwidth nonvolatile memory for xPU. High quality $HfZrO_2$ can be grown by ALD, where HfO_2 and ZrO_2 are alternatively grown layer by layer. After crystallization anneal, $HfZrO_2$ becomes orthorhombic phase and shows ferroelectricity. We found that OS capping layer helps to reduce anneal temperature and improves memory reliability. We demonstrated 1T1C FeRAM cell operation by Sn-doped IGZO (IGZTO) access transistor and HZO FE-capacitor with just 400℃ thermal budget [3].

(2) 3D vertical channel FeFET for high-density and low power FE storage memory.

Ferroelectric FET (FeFET) is an one-transistor memory device with FE gate insulator. Depending on its polarization, FET can be set as high V_{th} state or low V_{th} state. Similar to NAND flash memory, FeFET can also have 3D vertical channel architecture. We are interested in OS channel material instead of conventional poly-silicon channel for 3D FeFET because of its high mobility, low thermal budget, and potentially high reliability. We developed ALD growth process of InOx and applied it to 3D vertical channel FeFET integration process. We demonstrated memory operation of 3D vertical channel FeFET with 5nm-thick InOx [4].

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8:30am **AA1-WeM-3 Cross-Point Metal-Ferroelectric-Metal Capacitors Array for Compute-in-Memory Applications***, **Minjong Lee**, H. Hernandez-Arriaga, J. Kim, J. Kim,* University of Texas at Dallas

Rapid advancement of electronic technology has been a driving force towards the development of high-density and low-power processors, from a classical von-Neumann computing architecture to an interesting compute-in-memory (CIM) configuration. With the adoption of ferroelectric (FE) materials for CIM applications, most researchers have focused on the FE field-effect-transistors based vector-matrix multiplication (VMM) operation which can realize the analog conductance states;[1] however, the studies for metal-FE-metal (MFM) structure are rare to see.

In this work, we demonstrate a 2×2 pattern recognition system using a 4×2 cross-point array configuration of $Hf_{0.5}Zr_{0.5}O_2$ (HZO) MFM capacitors. TiN/HZO/TiN MFM capacitors were fabricated following our previous work.[2] However, the finger shaped TiN top and bottom electrodes (TEs and BEs) were patterned by the photolithography and ICP metal etching, and the thicker TEs were adopted to reduce series resistance components in TE lines. Since the polarization-change in MFM capacitors induces the different amounts of stored charges, the current signal can allow binarized states, generally called as switching and non-switching currents. It should be noted that the feature of HZO MFM capacitors is particularly similar to a polarization-induced synaptic charge behavior unlike conventional resistance/capacitance ones. Furthermore, the devices enable an excellent VMM operation, eligible for the neuromorphic computing with binary weight, by implementing the readout of maximum current value. For the pattern recognition, we followed the experimentally demonstration-method of 2×2 pattern recognition, introduced in a previous report.[3] Each cell of 2×2 pattern was applied to the TiN TEs, in which the white pattern is regarded as positive polarization state by 2.5 V set-pulse while the black pattern implies a negative polarization state by –2.5 V set-pulse. The tested patterns are all occurrences in 2×2 patterns (total 16 patterns). As the pattern recognition results, the current readout has the recognition accuracy of 81.3%, which is comparable results with the previous report,[3] thus highlighting the promise of the simple MFM capacitors towards the neuromorphic computing applications. The detailed results will be presented.

This work is supported by GRC-NMP program (#3001.001) of SRCUT Dallas' Texas Analog Center of Excellence (TxACE). The ozone generator used in this work was provided by TMEIC.

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8:45am **AA1-WeM-4 Using ALD to Precisely Place Multiple Transition Metal Impurities to Defect Engineer MIM Diode Performance***, **Shane Witsell**, J. Conley,* Oregon State University

Metal/insulator/metal (MIM) diodes promise ultra-fast rectification for applications in THz energy harvesting and detection but simultaneously require low turn on voltage (V_{ON}), low zero bias resistance (ZBR), and reasonable current-voltage (*I-V*) asymmetry (f_{asym}). Methods for improving these parameters beyond the standard use of different work function metal electrodes ($\Delta\Phi_M$), include multiple insulators (MIIM, MIIIM) to promote resonant or "step" tunneling, geometric field enhancements (using, e.g., carbon nanotubes), and *intrinsic* defects to promote defect-enhanced conduction [1]. Recently, we applied atomic layer deposition (ALD) to precisely insert transition metals into the Al_2O_3 tunnel barrier of dissimilar electrode MIM diodes. These metals introduce *extrinsic* defect levels that enable conduction pathways not present in undoped Al_2O_3 [2]. Ni (D_{Ni}) defects placed nearer the smaller Φ_M electrode, improved f_{asym}, but increased V_{ON}, likely due to negative charge trapped at defect levels lying energetically near or below the equilibrium Fermi level ($E_{F,equil}$) of the electrodes [3]. On the other hand, Ti (D_{Ti}) defects placed near the larger Φ_M electrode reduced V_{ON} due to positive charge trapped in levels above $E_{F,equil}$, but slightly increased f_{asym}. Results were consistent with asymmetric trap assisted tunneling (TAT). In this work, both Ni and Ti impurity defect layers were inserted at specific positions within the Al_2O_3 insulator thickness to allow for defect levels to align at specific applied voltages to promote asymmetric dual defect assisted tunneling.

ALD was performed using TMA/H_2O, Ni(tBu$_2$DAD)$_2$/O_3, and TTIP/H_2O. Two versions of doped structures were created: (i) "Dual Doped" in which the two ALD cycle Ni defect layer was positioned within the Al_2O_3 closer to the smaller Φ_M electrode and the two ALD cycle Ti layer inserted near the higher Φ_M electrode, and (ii) "Reverse Doped" in which the positions of the Ni and Ti layers were swapped. Electrode pairs with varying work functions were tested to investigate defect alignment. The Dual Doped Pt/Al_2O_3/Al produced the largest increase in low voltage asymmetry over undoped MIM devices, while the Reverse Doped Pt/Al_2O_3/Al device produced higher breakdown voltages and high voltage asymmetry. Both devices show lower ZBR. Additional results will be presented at the meeting including capacitance-voltage measurements on MIM and metal/oxide/semiconductor (MOS) devices. This work shows that ALD can be an effective tool for engineering device behavior.

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3. Holden *et al. J. Appl. Phys.* 129,144502 (2021).

9:00am **AA1-WeM-5 The Impact of Oxygen Source on the Formation of TiN Interface at the Initial Stage ALD process of Hafnia-based Ferroelectrics: An *in-situ* Analysis***, **Jin-Hyun Kim**, S. Kim, D. Le, Y. Jung, S. Hwang, H. Hernandez-Arriaga, M. Lee, A. Khosravi, K. Tan,* University of Texas at Dallas*; J. Spiegelman, M. Benham,* RASIRC*; S. Kim,* Kangwon University, Republic of Korea*; J. Kim,* University of Texas at Dallas

Ferroelectricity in doped hafnia is widely studied with its promising capability for memory applications. However, despite the mature HfO2 ALD technology, hafnia-based ferroelectrics still have major reliability issues such as relaxation, imprint, fatigue, and breakdown.1 These reliability properties are deeply related to the interface condition between the ferroelectric film and the electrodes. Thus, many reports suggested ways to improve reliability and enhance ferroelectricity by modifying the interface states of the metal-ferroelectric-metal (MFM) capacitors.2 Furthermore, the interface becomes a bigger issue for the ferroelectric layer scaled down thinner than 5 nm due to series capacitance and difficulties in crystallization

due to high surface energy.3 Therefore, it is crucial to understand the interface formation and the properties more carefully to further improve the reliability and scalability of the hafnia-based ferroelectric materials.

Herein, we investigated the effects of various oxidants on the interface layer using in-situ reflectance absorption infrared spectroscopy (RAIRS) and X-ray photoelectron spectroscopy (XPS). With these techniques, we monitored the surface reactions and interface formation in Hf0.5Zr0.5O2 (HZO) ALD process with TDMA-Hf/Zr and three different oxidants sources (H2O, O¬3, and anhydrous H2O2) on TiN substrate at 250 °C. As determined with in-situ IR absorbance spectra, all three oxidants effectively oxidized the TiN surface with just 1 exposure cycle. With additional pulses of O3, the intensity and peak area of features related to Ti–O and TiN–O continuously increased. However, in the case of H2O and H2O2, limited formation of oxygen bonds was observed on TiN surface. Interestingly, contrasting to H2O, H2O2 formed self-limiting peroxyl groups on the TiN surface with a minimum interface formation, resulting in superior film properties and robust reliability of H2O2-based HZO capacitors.

Moreover, the in-situ XPS data using H2O showed the formation of Ti–O bonds after the initial cycle more clearly, which strongly supports the RAIRS result. Extensive in-situ XPS analysis will be conducted to confirm these observations in the IR spectra.

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[1] J. Mohan et al., ACS AELM, 4, 4 (2022).

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[3] H. Lee et al., ACS AMI, 13 (2021).

9:15am **AA1-WeM-6 Performance Enhancement in HZO Based Ferroelectric Memory Devices***, **Ranjith K. Ramachandran**, L. Lukose,* ASM Belgium*; A. Leonhardt, M. Surman,* ASM Microchemistry Ltd., Finland*; V. Koladi Mootheri,* ASM Belgium*; M. Ioana Popovici,* IMEC, Belgium*; M. Givens, A. Illiberi,* ASM Belgium

HfO_2 based ferroelectric (FE) materials have gained tremendous attention as a potential candidate for memory applications such as FeFET and FeRAM. Since its first demonstration as a FE material [1], immense research has been done to circumvent the challenges such as scalability, increasing the remnant polarization (Pr), and improving endurance. Among others, Zr-doped HfO_2, hafnium zirconate (HZO) is being intensively studied due to its compatibility with complementary metal oxide semiconductor (CMOS) processing and excellent scalability.

The ferroelectricity in HZO films is believed to originate from the presence of polar metastable orthorhombic phase (o-phase: Pca21). Several methods have been explored to stabilize o-phase in the films, such as annealing, doping, and interface engineering. This, in turn, depended on the advent of synthesis methods that offer atomic level control over the thickness, composition, and interface, i.e., Atomic Layer Deposition (ALD). In this report, using ALD, we demonstrate three different methods such as 1) precursor selection 2) doping, and 3) interface engineering to improve the FE performance of HZO. ALD of HZO and La:HZO films was performed in a 300mm, industrial scale, EmerALD ALD reactor at a substrate temperature of 275^oC. Both halide and MO-based precursors were used as the metal source with H_2O/O_3 as a co-reactant and their FE performances were compared via remanent polarization (2Pr) and endurance measurements.

First, the influence of ALD precursor and co-reactant on the performance of HZO devices is demonstrated. Halide-based precursor shows initially high 2Pr compared to the MO (with O_3 as co-reactant). However, the onset of fatigue is at $1x10^5$ cycles due to the presence of possible Cl impurities. In the case of MO precursor, there is an observed wakeup effect which can be attributed to the transition from the tetragonal-orthorhombic phase (t-o phase) to the stable o-phase with increased cycling. The stable o-phase leads to higher 2Pr with the number of cycles and better endurance (fatigue at $3.5x10^7$ cycles) compared to the halide-based precursor (**Fig. 1**). Together with low coercive field (2Ec) and high 2Pr, this MO-based process has useful applications in Fe-RAM. In addition, ozone as co-reactant shows improved 2Pr compared to water.

Furthermore, La doping on HZO was carried out to improve wake-up, max 2Pr, and endurance (Table 1). Subsequently, interface engineering with La-doped HZO resulted in record-high 2Pr (63 $\mu C/cm^2$), with high endurance and lower wake-up (**Table 1**) [2].

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9:30am **AA1-WeM-7 Stabilization of Tetragonal Phase of Ti-doped ZrO_2 Deposited by ALD***, **Seokhwi Song**, Y. Choi, E. Kim, K. Kim, H. Jeon,* Hanyang University, Korea

Manufacturing metal-insulator-metal (MIM) capacitors with high capacitance and low leakage current for dynamic random access memory (DRAM) has become a challenge as electronic devices rapidly decrease in size and distances between devices increase. Therefore, in this study, Ti-doped ZrO2 was investigated as a high-k material for DRAM capacitors. ZrO2 film has been widely studied as a high-k material for DRAM capacitors due to its high permittivity and wide bandgap. ZrO2 has monoclinic, cubic and tetragonal crystal phases. The dielectric constant of ZrO2 is highly dependent on the crystal structure (monoclinic: 19.7, cubic: 36.8, tetragonal: 46.6). However, a material with a higher permittivity than common ZrO2 was required, and a method of changing the crystal structure of ZrO2 through doping was studied. The same tetravalent element as Zr can stabilize the cubic/tetragonal phase of ZrO2 without introducing oxygen vacancies into the thin film. When the tetravalent dopant is replaced by a Zr atom, the distance between the dopant and the O atom is different from that of the Zr-O atom, so it is converted into a cubic or tetragonal phase. Among them, Ti dopant is a promising stabilizer to replace Zr atoms.

Atomic Layer Deposition (ALD) is an optimal deposition method for Ti-doped ZrO2 at a desired Ti dopant concentration. The concentration of Ti may be controlled through a super cycle ALD process in which n ALD cycles for the host material ZrO2 and 1 ALD cycle for the dopant material Ti are repeated. Through this ALD process, Ti-doped ZrO2 having a desired doping concentration can be deposited to a desired thickness. Ozone with high oxidizing power is essential to improve crystallinity. Since the crystallinity varies not only with the dopant concentration but also with the ozone concentration, Ti-doped ZrO2 is deposited at various ozone concentrations of 100 to 400g/m3 to check the crystallinity change.

In this study, Cyclopentadienyl Tris(dimethylamino)zirconium (CpZr(NMe2)3) was used as a precursor and titanium isopropoxide (TTIP) was used as a dopant. And ozone was used as a reactant. You want to deposit Ti doped ZrO2 and analyze the film with a supercycle ALD process. The core of this study is to confirm the change in the crystallinity of the thin film and the change in the physical properties of the thin film according to the Ti doping concentration.

9:45am **AA1-WeM-8 Three Terminal Synaptic Devices Employing ALD Grown Dual Dielectrics and Their Linear Learning Process***, **Jung Wook Lim**,* Electronics and Telecommunications Research Institute, Republic of Korea*; J. Kim,* ETRI, Republic of Korea

To overcome the limitation of the von-neumann architecture, synaptic devices has been widely researched to emulate synaptic functions[1-2]. For this, synaptic devices with high stability and CMOS compatibility are required to overcome the barrier of commercial entry. Three terminal inorganic oxide transistors may be most suitable to satisfy these requirements. In our group, three terminal synaptic transistors employing ALD grown the TiO_2 channel layer and dual gate dielectrics were fabricated on Si n^{++} wafers (used as bottom gate electrodes) and the vertical structure is shown in Fig. 1. The synaptic behavior is performed by storing or capturing charges, and for this purpose, the interface trap sites were formed at the interface between channels and dielectrics by in-situ ALD process. We have used selectively deep traps among traps at different levels in the energy bandgap for capturing holes, resulting in negative shift of threshold voltages[3-4]. As a synapse device in which learning is performed by an electrical signal, a phenomenon in which the transfer curve moves in a negative direction by hole traps was observed after supplying an electrical pulse. Interestingly, when a voltage pulse of 10 V or higher is applied for 0.5 s, the conductivity increases abruptly and the metallic behavior was observed and the result is shown in Fig. 2. For confirming synaptic performance, paired pulse facilitation (PPF) curves were obtained, in which 0.4 s and 11.11 s of life times were obtained for the pulse times of 5 ms and 0.5 s (10 V), respectively. With electrical pulses

of 10 V and 3 ms of short-term plasticity condition derived from PPF curves, long term plasticity was obtained with repeated pulses and the results are shown in Fig. 3. The 1024 conduction states (10 bit) was obtained with high linearity, which implies the high accuracy of recognition. The dual dielectrics are composed of ALD grown SiOx and AlOx films. The deep trap sites were formed at the interface of SiOx and TiO_2 channel layer, hence indicating that the in-situ plasma treatment is very important during the ALD growth. The AlOx films confirms the stability of devices and enhances the performance of transistors. In the further study, synaptic devices will implement the forgetting curves of human brains and their various phenomena.

References

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