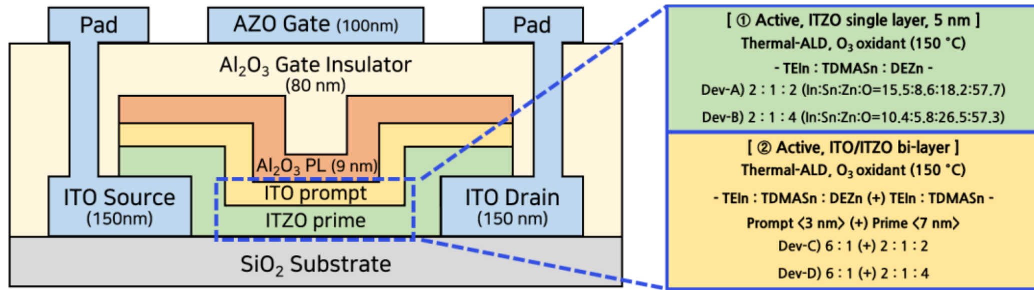

Figure 1. Schematic cross-section of the fabricated TFTs employing the ITO/ITZO bilayer channel configurations with overall process conditions including sub-cyclic ratios of ALD super-cycles for the preparation of active channel layers.

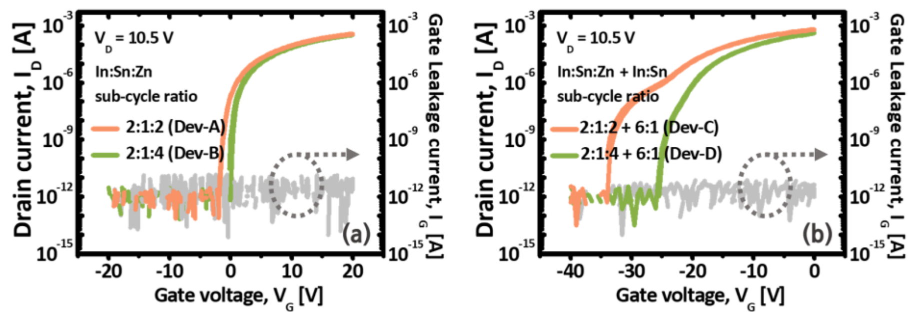

Figure 2. Comparisons in transfer characteristics and gate leakage currents (a) between two single-layer ITZO TFTs (Dev-A and Dev-B) and (b) between two bi-layered ITO/ITZO TFTs (Dev-C and Dev-D).

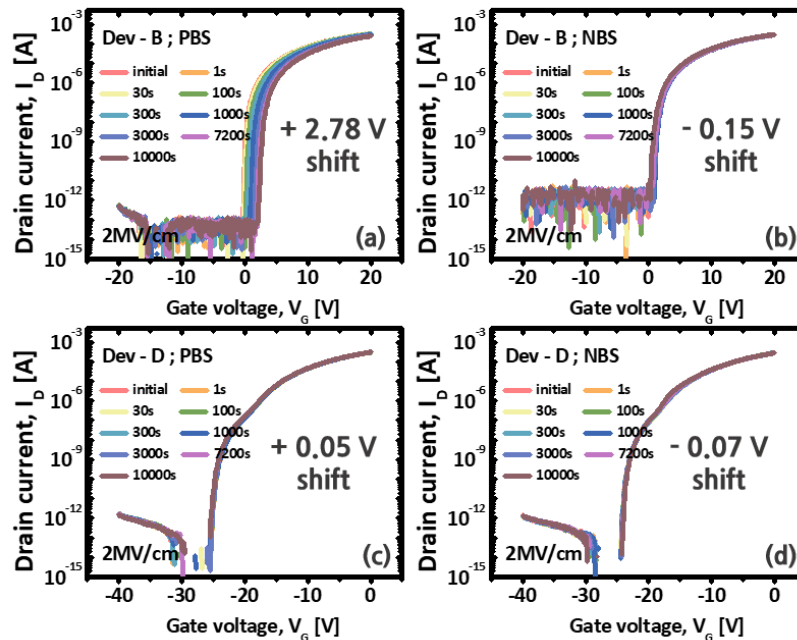

Figure 3. Variations in transfer curves with stress time evolution for the Dev-B under (a) PBS and (b) NBS, and for the Dev-D under (c) PBS and (d) NBS. For the PBS or NBS tests, the gate bias stress of +20 or −20 V was applied for 10^4 s, respectively, and the V_{DS} was set at 10.5 V.