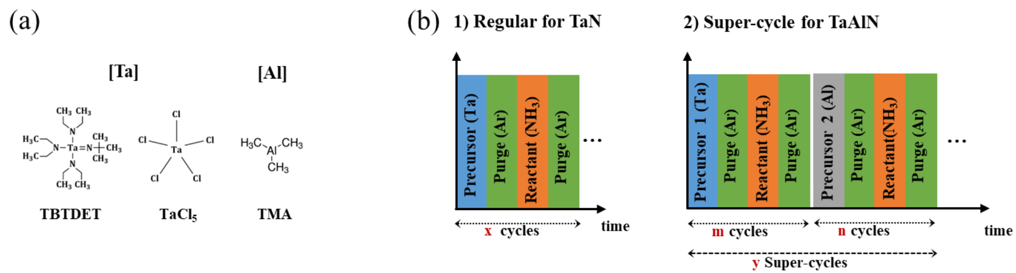

Figure 1. (a) Metal precursor types in this study (b) ALD process sequences for metal gates.

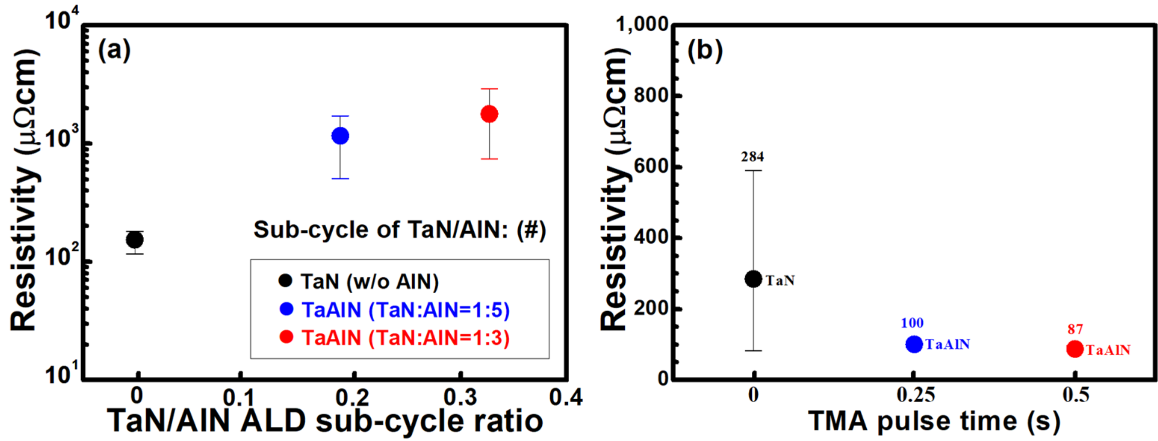

Figure 2. The resistivity is confirmed in the fabricated metal gate electrodes with 5 nm thickness on Si substrates (a) with varying ALD sub-cycle ratios of TaN/AlN (b) different TMA pulse time in ALD process.

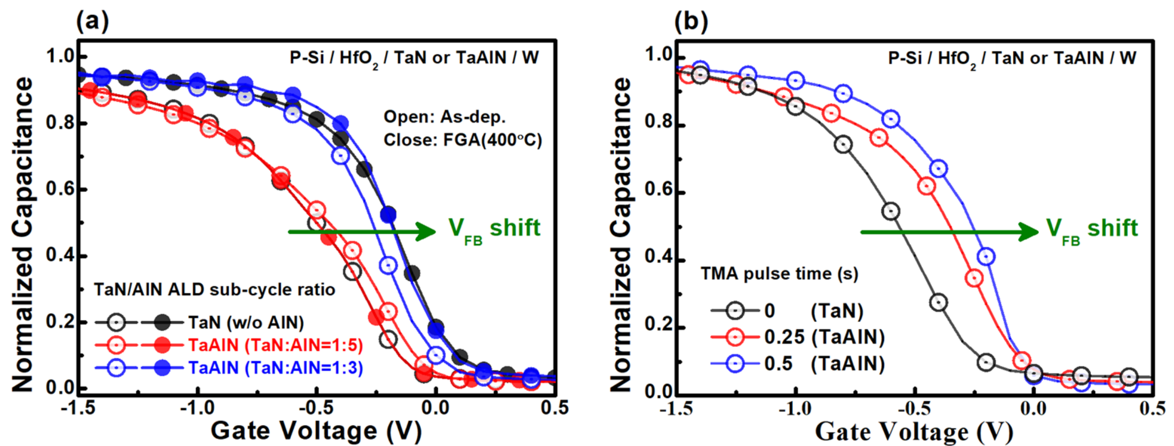

Figure 3. Normalized *C-V* characteristics of MOS capacitors (a) with varying ALD sub-cycle ratios of TaN/AlN (b) different TMA pulse time in ALD process.

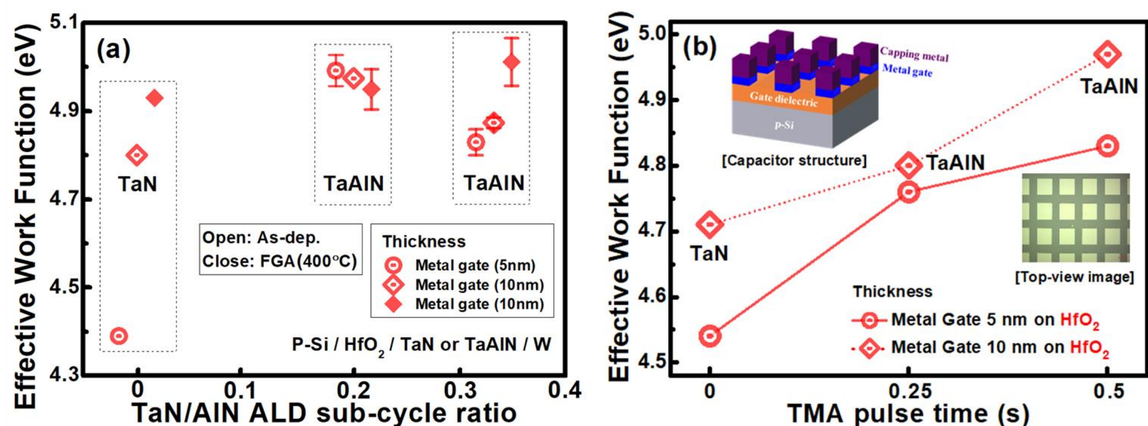

Figure 4. The modulated effective work function of TaN & TaAlN metal gate stacks (a) with varying ALD sub-cycle ratios of TaN/AlN (b) different TMA pulse time in ALD process.