ALD Applications
Room Tamna Hall A - Session AA-TuA

3D Semiconductor Devices
Moderators: Dennis Hausmann, Lam Research, **Reza Jafari Jam**, AlixLabs

1:30pm **AA-TuA-1 Characteristics of ALD IGZO for the application in Stackable DRAM Cell***, Seung Wook Ryu,* R&D Process, R&D division SK hynix Inc, Republic of Korea **INVITED**

This study aims to address the availability of Atomic Layer Deposited InGaZnO (ALD IGZO) as the stackable channel for the application in DRAM (Dynaic Ramdom Access Memory) cell.

The memory industry has grown significantly in response to the changes in the computing environment following the personal computer to artificial inteligence

(AI) era. The need for data creation, storage and processing will increase exponentially with the expansion of AI computing, much more rapidly than the traditional amount of data increase. As DRAM physically arrives at sub ten nanometer scale, the issues been more serious in many aspects, such as patterning for high aspect ratio structure, high-k material innovation as capacitor dielectric, resistance of gate material and so on.

The conversion to new platform is one of promising candidates to overcome current physical limits of DRAM and new channel material is a key component to realize new DRAM platform. IGZO is one of promising candidates as new channel material for DRAM cell transistors.

After physical properties of PVD IGZO related to electrical properties are investigated as the reference, those of ALD IGZO will be compared and then, hydrogen effect from precursor and integration will be presented.

Finally, we are going to check out the properties of ALD IGZO as compared with that of PVD IGZO and discuss the possibility as new form factor.

2:00pm **AA-TuA-3 5 nm Thick Indium Nitride Channel Layers Fabricated by PEALD for 3D Transistor Architectures***, Doo San Kim, Minjong Lee, Min Gyeong Jo, Thi Thu Huong Chu, Dushyant Narayan, Dan N. Le,* The University of Texas at Dallas*; Youngbae Ahn, Ja-Yong Kim, Seung Wook Ryu,* SK hynix, Republic of Korea*; Jiyoung Kim,* The University of Texas at Dallas

As Si channel scaling continues, highly complex 3D transistor architectures, such as complementary FETs (CFETs) and vertical FETs, are emerging. Alternative channel materials, such as two-dimensional transition metal dichalcogenides (2D TMDs) and indium gallium zinc oxide (IGZO) semiconductors, have garnered significant attention as potential replacements for conventional Si channel layers.However, these alternative materials must meet extremely challenging requirements, including high effective field mobility, high drive current, and a large on/off current ratio, while enabling 3D structure Si device compatible process and ensuring channel thickness scalability down to sub-5 nm. Among the promising candidates, indium nitride (InN) stands out due to its high electron mobility (~3,600 $cm^2/V{\cdot}s$), peak electron velocity exceeding 2×10^8 cm/s, and an appropriate bandgap greater than 0.75 eV [1,2].

Despite its potential, there are limited reports on InN-based transistors fabricated by atomic layer deposition (ALD), likely due to the challenges associated with growing sub-10 nm thick films with reliable electrical characteristics at low deposition temperatures. These difficulties stem from the low reactivity of In precursors with NH_3, relatively weak In-N binding energy, contamination from carbon and hydrogen, and challenges in achieving conformal deposition. Additionally, while InN films thicker than 10 nm typically exhibit metallic behavior due to high electron concentration, ultra-thin InN layers are expected to exhibit semiconductor properties.

In this presentation, we report the deposition of sub-5 nm conformal InN films using Hollow-Cathode Plasma (HCP)-enhanced ALD and evaluate their performance in back-gated thin-film transistor (TFT) devices. We examine the impact of process conditions—including plasma power, working pressure, and deposition temperature—on film characteristics. InN layers were deposited at 280°C on a 15 nm–100 nm SiO_2 back-gate dielectric atop a Si substrate. After defining the TFT channel, source/drain contacts were patterned.We presented InN TFT results, including transfer and output characteristics, temperature dependence, and channel length scaling. Our findings demonstrate that InN-based TFTs with a 4 µm channel length achieve an on-current of ~50 µA/µm, an I_{on}/I_{off} ratio exceeding 10^6, and a field-effect mobility of ~10 $cm^2/V{\cdot}s$ at $V_D = 5$ V.

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[1] Imran, A., et al. *Adv.Mater.Interfaces* **10**, 2200105 (2022).

[2] Oseki, M., et al, *Sci. Rep.* **4**, 3951 (2014).

2:15pm **AA-TuA-4 Bottom-Up Mo Fill for Metal Interconnect Applications: Selective and Superconformal Approaches***, David Mandia, Matthew Griffiths, Arya Shafiefarhood, Justin Kim, Aleksandr Plokhikh, Youness Alvandi, Nick De Marco, Ben Natinsky, Andrew Melton, Jennifer O'Loughlin,* Lam Research Corporation

As devices continue to scale down to <2nm node, chip suppliers recently started replacing current metals (e.g., copper) with alternative metals due to reduction in current-carrying cross-section, increase in electron scattering, and integration challenges in narrow features. While cobalt (Co) and ruthenium (Ru) are attractive options for resistivity scaling and as middle-of-the-line (MOL) interconnect materials, they require the use of liners and are not amenable to downstream CMP processing. Selective (i.e., bottom-up) molybdenum (Mo) deposition represents a transformative approach to addressing the challenges of void-free filling in high-aspect-ratio structures for semiconductor manufacturing. Mo is a promising alternative to tungsten (W) in MoL applications where the CD of the via is below 15nm. However, achieving large grain Mo growth in complex geometries requires precise control over the deposition process and the use of a well-suited precursor.

This work focuses on $MoO_aX_b(L)$, a family of key precursors due to their unique ability to modulate between etching properties, selective deposition, or conformal deposition, depending on process design & substrate. Because some substrates do not lend themselves well to selective Mo deposition, we developed superconformal Mo deposition strategies so that we could achieve large-grain growth on any substrates and structures.

The proposed void-free Mo fill approaches take two different paths to achieve the same goal:

1. Selective Mo Deposition: Where the Mo inherits its selectivity from the substrate. Highly selective for certain applications but limited by substrate architectures.

2. Superconformal Mo Deposition: Where the bottom-up growth is controlled by the deposition kinetics and is derived from a conformal process. This can be tuned to fill any via or trench over a wide range of aspect ratios and is independent of the material at the bottom of the feature.

Extensive characterization using advanced microscopy techniques, including PED, TEM and EDX, confirms the deposited Mo films' superior quality, showcasing excellent conformality and absence of seam voids, even in features with reentrant profiles. These findings address many of the grand challenges for low resistance interconnects. The insights presented provide critical guidance for future material innovations and process optimization in semiconductor manufacturing.

Keywords: Bottom-up Mo fill, $MoO_aX_b(L)$, selective deposition, ALD, semiconductor manufacturing

2:30pm **AA-TuA-5 Thermal Atomic Layer Deposition of Sn-incorporated MoO_2 Electrode Films for High-performance TiO_2-based DRAM Capacitors***, Jae Hyeon Lee, Jeong Hwan Han,* Seoul National University of Science and Technology, Republic of Korea

As dynamic random access memory (DRAM) capacitors continue to downscale, the demand for new electrode materials to improve device performance has increased. Titanium nitride (TiN), a conventional electrode for DRAM capacitors, is approaching its limits due to its low work function and chemical instability at the interface. To overcome these limitations, molybdenum dioxide (MoO_2) has emerged as a promising alternative, as it offers a high work function (>5 eV) that helps suppress leakage current and exhibits excellent stability at the interface with high-k dielectric materials. Notably, its structural similarity to rutile TiO_2 enables the low-temperature crystallization of high-k rutile TiO_2. However, the formation of monoclinic MoO_2 presents challenges, as it is a metastable phase with a higher formation energy than the stable MoO_3 phase. Although numerous studies have explored the fabrication of monoclinic MoO_2 films using a range of deposition methods, including pulsed laser deposition, reactive sputtering, and chemical vapor deposition, these techniques are unsuitable for DRAM capacitor fabrication due to the requirement for conformal growth on a three-dimensional substrate with an exceptionally high aspect ratio.

In this study, a simple thermal atomic layer deposition (ALD) process was developed to grow monoclinic MoO_2 films. It was found that the metastable MoO_2 phase was stabilized by SnO_x incorporation in MoO_x due

to the template effect between SnO_2 and MoO_2. The electrical conductivity, surface morphology, and thermal stability of ALD SnO_x-incorporated MoO_x (TMO) films, as well as their interfacial properties with TiO_2 dielectrics, were evaluated to assess their potential as electrodes in TiO_2-based metal−insulator−metal (MIM) capacitors. ALD TiO_2 films grown on TMO exhibited remarkably suppressed leakage current and enhanced dielectric constants (>100), indicating that monoclinic ALD TMO facilitates the in situ crystallization of rutile TiO_2. These findings suggest that ALD TMO films are promising electrode materials for TiO_2-based MIM capacitors in advanced DRAM devices.

2:45pm **AA-TuA-6 Highly Ordered Crystalline ALD-InGaO Thin Films with High Mobility and Thermal Stability for Next-Generation 3D Memory Devices**, ***Seong-Hwan Ryu***, *Hye-Mi Kim, Dong-Gyu Kim, Jin-Seong Park,* Hanyang University, Korea

Recently, interest in atomic layer deposition(ALD)-derived oxide semiconductors (OSs) as a new channel of memory devices has increased dramatically to overcome scaled-down limitations. However, conventional amorphous OSs such as In-Ga-Zn-O are constrained by limitations such as degradation of field-effect mobility and low-phase stability during subsequent high-temperature processes, which are inevitable in memory devices. In this regard, thermally stable OSs with high mobility are required, and highly ordered crystalline OSs are emerging as leading examples. The representative material is In-Ga-O (IGO), doped with Ga to lower the oxygen vacancies in In2O3 with excellent crystallinity and low effective mass. However, in most cases, trimethylgallium is the only Ga source adopted for ALD, and the close distribution of dopants resulting from its small molecular size ultimately leads to a deterioration in crystallinity. This study presents a process to obtain highly ordered and thermally stable crystalline IGO thin films by ALD with bulkier gallium precursor. Through this, we suggest the optimal cation composition (In:Ga=4:1) with extremely high field-effect mobility (128.2 cm2/Vs) using IGO as the channel material in a thin film transistor and the impact of crystal structural changes on various film properties. An in-depth study of the IGO crystal structure suggests that the alignment degree of the cubic (222) planes is directly related to electrical performance and thermal stability. Also, process-wise, its excellent step coverage (side: 96%, bottom: 100%), compositional uniformity in a 40:1 aspect ratio structure, and superior crystal growth in vertical structures make it a promising candidate for application as a channel in next-generation 3D memory devices

3:00pm **AA-TuA-7 Amino Acid-Based BiomimeticOrganic-Inorganic Hybrid Memristors by Molecular Layer Deposition for Neuromorphic Applications**, *Lin Zhu,* ***Ai-Dong Li***, *Song Sun,* Nanjing University, China; *Yan-Qiang Cao,* Nanjing University of Science and Technology, China

With the rapid development of artificial intelligence, the need to mimic biological functions has become increasingly important so as to perform complex tasks under complicated external environments. Memristors have emerged as an extremely competitive candidate for neuromorphic artificial electronic devices owing to their biological-like capabilities. It is urgent to develop new memristive materials and architecture to meet diverse demands in artificial intelligence and neuron network systems.

In this study, drew inspiration from neurotransmitters in the human brain, we selected essential amino acids cysteine (Cys) as organic precursor to construct biomimetic titanium-based cysteine hybrid films via molecular layer deposition (MLD). The stability of the hybrid films was extensively examined, demonstrating excellent durability in both water and air. A vertically integrated single-layer Pt/Ti-Cys/TiN device exhibits reproducible volatile switching behavior, with gradual changes observed during the set/reset process. Notably, the device successfully emulates bio-pain sensation and synapse functions, indicating that these biomimetic hybrid films hold great potential for the development of artificial sensory systems.

The organic-inorganic hybrid materials possess abundant physical/chemical properties and unique merits from combination of both components, enabling great potential in flexible devices due to tunability and versatility in tailoring material structures and properties. To further optimize and regulate its performance, the bilayer-structured ultrathin memristor Pt/Al-Cys/Ti-Cys/TiN was prepared. The introduction of Al-Cys improves the device's resistive switching and retention characteristics, showing repeatable nonvolatile bipolar switching with an on/off ratio greater than 10^2. Some crucial bio-synaptic functions, such as long-term potentiation, long-term depression, paired-pulse facilitation, spike rate-dependent plasticity and pattern recognition were also realized in this device. Our results indicate the great potentials of MLD derived amino acid-based biomimetic hybrid memristor for flexible robust neuroscience applications.

3:15pm **AA-TuA-8 Design of Crystalline InGaO Channels with High-Temperature Stability via Thermal ALD Process Parameter Variations**, ***Hye-Jin Oh***, Hanyang University, Korea; *Dong-Gyu Kim,* Hanyang University, Republic of Korea; *Tae Woong Cho, Hae Lin Yang,* Hanyang University, Korea; *Jihyun Kho, Yurim Kim, Bong Jin Kuh,* Samsung Electronics Co., Republic of Korea; *Jin-Seong Park,* Hanyang University, Korea

Oxide semiconductors have garnered interest as potential materials to address the issues caused by the scaling down of dynamic random-access memory devices.[1] However, high-temperature stability is a critical requirement for applying oxide semiconductors to memory devices.[2] To overcome the challenges of high-temperature instability in oxide semiconductors, it is essential to maintain a similar crystal structure regardless of the annealing temperature. Here, we proposed an optimized crystalline InGaO (IGO) film for high temperature stability by engineering atomic layer deposition process parameters, ozone concentration, and deposition temperature. Our results reveal that high-temperature stability can be secured by using elevated ozone concentrations and deposition temperatures in IGO deposition. Notably, IGO deposited at 300℃ shows little change in the main (222) intensity when annealed at 700℃ compared to 400℃, and a highly c-axis aligned (222) plane is observed. The field-effect transistor with an IGO active layer deposited at 300℃ showed minimal changes in electrical parameters after annealing at 700℃ (μ_{FE}: 58.4 to 68.7 cm^2/Vs) and demonstrated excellent PBTS stability (ΔV_{th}: 0.15 V) at 3 MV/cm, 95℃. These outcomes suggest the possibility of utilizing oxide semiconductors in memory devices that require managing high-temperature thermal budgets.

References

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