ALD Applications
Room Tamna Hall A - Session AA-MoA

Memory Applications I

Moderators: Hanmei Choi, Samsung Electronics, **Robert Clark**, TEL Technology Center, America, LLC

4:00pm **AA-MoA-11 Atomic Layer Technology for Ferroelectrics and Resistive Switching Devices: Advances in Epitaxial Growth, Doping, and Defect Control**, ***Miin-Jang Chen***, *Yu-Sen Jiang, Ting-Yun Wang, Chen-Hsiang Ling,* Department of Materials Science and Engineering, National Taiwan University, Taiwan **INVITED**

Atomic layer deposition (ALD), atomic layer epitaxy (ALE), and atomic layer annealing (ALA) have emerged as critical techniques for precise material engineering in advanced electronic devices, particularly for ultrathin ferroelectric and resistive switching materials in memory and energy storage applications. This presentation addresses two key areas: (1) ferroelectric/antiferroelectric materials, and (2) resistive random access memory (RRAM) devices. In the first area, novel ALD/ALE methods enable precise control of doping, crystallographic orientation, and domain dynamics in sub-10 nm ferroelectric films. The alternating multi-pulse ALD technique achieves homogeneous Zr doping in HfO_2, thereby enhancing ferroelectricity even at high Zr/Hf ratios. Monolayer engineering via atomic layer substitution in $Hf_{0.5}Zr_{0.5}O_2$ (HZO) significantly enhances the ferroelectricity at a thickness of only ~4 nm with nearly wake-up-free behavior. Epitaxial HZO films grown by ALE demonstrate record high ferroelectric polarization ($2P_r$ = 78.9 μC/cm^2) and ferroelastic domain switching correlated with time-resolved negative capacitance. Furthermore, antiferroelectric ZrO_2/TiN heterostructures achieve exceptional energy storage density (~118.6 J/cm^3) through orientation-controlled epitaxy. In addition, hydrogen-mediated ALE allows for low-temperature (300ºC) epitaxial growth of twin-structured TiN electrodes. For RRAM devices, ALA dramatically improves resistive switching properties by tailoring nitrogen vacancies with monolayer precision in sub-4 nm AlN and SiNx layers. ALA reduces operating voltages, improves switching uniformity, and enhances endurance and retention. Spatial vacancy control via ALA stabilizes conductive filament formation, which reduces cycle-to-cycle variation. These results demonstrate ALD, ALE, and ALA as transformative techniques for next-generation nanoscale electronics, offering pathways toward high-performance memory and energy storage solutions.

4:30pm **AA-MoA-13 Atomic-Scale Processing of Ruthenium Thin Films via ALD and ALE for Advanced Interconnects**, *ChangHwan Choi,* ***YoungSeo Na****, HyunJin Lim, SangKuk Han, HyoJin Ahn, YehBeen Im, WonJae Choi,* Hanyang University, Korea

Ruthenium has been recognized as a next-generation interconnect material capable of overcoming the scaling limitations of copper interconnects. To effectively integrate ruthenium into complex three-dimensional semiconductor structures, precise control of atomic layer deposition (ALD) and atomic layer etching (ALE) processes is essential. In this study, we investigated the electrical and chemical properties of ruthenium thin films deposited at various temperatures via ALD to achieve low-resistivity ruthenium films. The optimized ALD-grown films were subsequently processed via ALE for precise thickness regulation.

The ALD-Ru process was performed in the temperature range of 225-375ºC using (ethylbenzene)(1-ethyl-1,4-cyclohexadiene)ruthenium(0) (EX03Ru) as the Ru precursor, with O_2 as the reactant. At the ALD window (375ºC), a high-quality ruthenium thin film with a very low resistivity (~20.3 μΩ·cm) and a growth per cycle (GPC) of 0.61 Å/cycle was achieved (Fig. S1). X-ray photoelectron spectroscopy (XPS) analysis confirmed that the content of non-conductive RuO_x decreased from 12.9% at 225ºC to 2.8% at 375ºC, leading to reduced resistivity (Fig. S2). In contrast, X-ray diffraction (XRD) results revealed that the film exhibited the highest crystallinity at 275ºC (Fig. S3). Additionally, post-deposition forming gas annealing was performed on the film deposited at 275ºC at the back-end-of-line (BEOL) thermal budget of 400ºC for 1 hour, resulting in a 72% improvement in resistivity, grain growth, and a reduction in surface roughness from an RMS value of 1.54 nm to 1.18 nm. Furthermore, a plasma-enhanced ALE process was developed to achieve uniform etching of the optimized Ru film. The ALE process consisted of two primary sequential steps: (1) surface modification via oxidation with O_2 plasma or fluorination with CF_4 plasma, forming a self-limiting modified layer on the surface, and (2) selective removal of the modified layer using low-energy Ar plasma. Through process optimization, the self-limiting nature of ALE was maintained even in high-aspect-ratio (12:1) structures, minimizing surface contamination and ensuring stable and uniform etching. These results confirm that ALD and ALE support the fabrication of high-performance thin films while enabling precise sub-nanometer thickness control and achieving reliable material processing, underscoring the potential of an integrated atomic-scale approach for next-generation interconnect technology.

4:45pm **AA-MoA-14 ALD of ferroelectric TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN stacks; growth and interfacial oxidation studied by *in situ* spectroscopic ellipsometry**, ***Stijn van der Heijden***, Eindhoven University of Technology, Netherlands*; Florian Wunderwald, Uwe Schroeder,* Namlab, Germany*; Marcel Verheijen, Erwin Kessels, Bart Macco,* Eindhoven University of Technology, Netherlands

Ferroelectric devices, particularly those based on $Hf_{0.5}Zr_{0.5}O_2$ (HZO), are a promising upcoming technology to enable high-speed, low-power computation.[1,2] However, for the successful implementation of these ferroelectric devices, several obstacles must be overcome. One such obstacle is the internal bias field, which – similarly to imprint – causes a shift in the coercive field making it more difficult to switch to the opposing polarization. The cause of this internal bias field is still subject to investigation, yet it is suspected to come from a defective interface between the metallic electrode and the ferroelectric material within the metal-ferroelectric-metal (MFM) stack. To form functional ferroelectric devices, the ability to accurately analyze the growth and interfacial formation of these MFM stacks is thus essential.

In this work, full TiN/HZO/TiN stacks were grown by ALD without breaking vacuum. For TiN, the used precursor was $Ti(NMe_2)_4$ and the co-reactant was a plasma containing a mixture of Ar and NH_3. For HZO, the used precursors were $CpHf(NMe_2)_3$ and $CpZr(NMe_2)_3$, and the co-reactant was either O_3 or an O_2 plasma. The growth of TiN and HZO in both nucleation and steady-state phases was measured using *in situ* spectroscopic ellipsometry. The film thicknesses for TiN and HZO were approximately 14 and 10 nm, respectively. Crucially, the oxidation of the bottom TiN electrode caused by plasma and ozone exposure when growing HZO – which is suspected to be a significant source of the internal bias field – could be investigated using ellipsometry. The TiN/HZO/TiN stacks were subsequently annealed and ferroelectric measurements were performed, confirming the suspected trend: increased interfacial oxidation leads to an increased internal bias field. Our studies thus show the capability of *in situ* ellipsometry to measure the growth and interfacial oxidation of TiN/HZO/TiN, aiding the optimization of the growth process of ferroelectric devices.

[1]J.P.B. Silva et al. APL Mater. 11, 089201 (2023)

[2]U. Schroeder, M.H. Park, T. Mikolajick, C.S. Hwang. *Nat Rev Mater* **7**, 653–669 (2022)

5:00pm **AA-MoA-15 Stable Synaptic Function and Orientation Selectivity Recognition Under Strain in Bilayer Stretchable Memristors via Atomic Layer Deposition**, ***Ying-Jie Ma***, *Ai-Dong Li,* Nanjing University, China

Memristors trigger enormous potentials in neuromorphic computing and advanced artificial intelligence due to their advantages in information storage and cognitive computation. However, the integration of memristors into flexible and stretchable devices, such as wearable health monitors, non-biological prosthetics, and soft robotics, suffers a tough challenge. Great efforts have been made on flexible memristors to meet the increasing demands, however report on stretchable memristors remains scarce. It is critical for ensuring the performance stability of stretchable devices under strain.

In this work, stretchable memristor of PDMS/Au/HfO_2/Al_2O_3/Ag was developed based on a discrete structural design. The discrete structure was achieved through sacrificial layer transfer and photolithography, with 10 nm Al_2O_3 and 10 nm HfO_2 functional layers deposited via atomic layer deposition (ALD), providing stable retention(up to 10^4 s) and reproducibility (100 cycles). Compared to conventional continuous designwithout photolithography, it exhibits a higher flexibility up to 30%. Under dynamic stretching and releasing, the device maintains stable resistive switching behavior and accurate replication of synaptic functionality. Even at 30% strain, the memristor's switching ratio remains at 10^3 and simulates a series of synaptic functions, including paired-pulse facilitation (PPF), long-term potentiation/depression (LT_P/LT_D), post-tetanic potentiation (PTP), short-term potentiation to long-term potentiation transition (STP-LTP), spike amplitude-dependent plasticity (SADP), spike width-dependent plasticity (SWDP), spike frequency-dependent plasticity (SRDP), and spike-timing dependent plasticity (STDP).

Furthermore, the threshold sliding effects, enhanced depressive effects (EDE), and orientation selectivity recognitionin Bienenstock-Cooper-Munro

(BCM) learning rule have been realized in our stretchable memristors by leveraging the memristor's history-dependent plasticity. This work provides a new structural and material framework for stretchable memristors, ensuring reliable performance in dynamic environments, which is vital for the next generation of flexible electronics.

5:15pm **AA-MoA-16 P-Type Tellurium Thin Film Transistor with Sacrificial Atomic Layer Deposition***, **Wonho Choi**, Byongwoo Park, Seungjae Yoon, Jeong Woo Jeon, Gwangsik Jeon, Sangmin Jeon, Sungjin Kim,* Seoul National University, South Korea*; Chanyoung Yoo,* Hongik University, Republic of Korea*; Cheol Seong Hwang,* Seoul National University, South Korea

A complementary thin film transistor (CTFT) has long been a desired device structure for monolithic three-dimensional integration architecture with the complementary metal oxide semiconductor (CMOS) field-effect transistors fabricated on a Si wafer surface[1]. They must also be compatible with the back-end-of-line conditions with limited thermal budgets (< 400 ^{o}C)[2]. The n-type TFTs with reasonable performances are available using amorphous oxide semiconductors. Still, the lack of p-type TFT (p-TFT) with comparable performance hinders the advancement of CTFT technology[3]. P-type two-dimensional transition metal dichalcogenides, such as WSe_2, have drawn attention for this application, but their flake-based process is incompatible with the standard CMOS processes[4]. Elemental tellurium (Te) is another candidate for p-type channel material due to its unique high hole mobility[5]. However, the reported fabrication processes are incompatible with the CMOS processes[6]. Another crucial issue is ensuring the channel material's intimate contact with the source and drain electrodes[7]. While the contact properties are fundamentally determined by the electron affinity of the channel material and contact metal work function, the metal-induced gap state adversely affects the Schottky barrier formation, pinning the Fermi level at an undesired position within the band gap[8]. Therefore, no CMOS-BEOL-compatible p-TFT devices have been reported regarding the fabrication process (low growth temperature and non-flake type) and electrical performance (comparable or even higher drive current density than the n-type counterpart).

This study introduces an innovative sacrificial atomic layer deposition (s-ALD) for crystalline Te film for p-TFT fabrication, which is required for monolithic three-dimensional device integration. It selectively grows p-type Te channel film on the gate insulator with its high hole mobility axis (c-axis) aligned with the electric current flowing direction (substrate surface direction) while forming a semimetal $NiTe_2$ interlayer on the Ni metal contacts for low contact resistance. The p-TFT device outperforms the previous works with 1.3 × 10^{-5} Aμm^{-1} on-current density, 40 $cm^2V^{-1}s^{-1}$ hole mobility, and 0.9 k$\Omega\mu$m contact resistance, which remained unaffected by atmospheric exposure over 250 days. Furthermore, the low deposition temperature of 80 ^{o}C and wafer-scale uniformity enhance its compatibility with CMOS technology.

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