ALD Applications
Room Tamna Hall A - Session AA1-TuM
Memory Applications II

Moderators: Pinyen Lin, TSMC, **Seung Wook Ryu**, SK hynix

8:00am **AA1-TuM-1 Effect of Ga Doping on Coercive Field Reduction and Endurance Enhancement in Atomic Layer Deposited HfO2-based Thin Film for FeRAM Applications**, ***Zi-Ying Huang***, *Yu-Chun Li,* Fudan University, China*; Ming Li,* Peking University, China*; Ye Zhu,* Hong Kong Polytechnic University, China*; David Wei Zhang, Hong-Liang Lu,* Fudan University, China

HfO_2-based ferroelectric memory (FeRAM) has emerged as a promising candidate for next-generation nonvolatile memories, owing to its remarkable compatibility with CMOS processes and scalability. However, the reliability of HfO_2-based materials remains a significant challenge, primarily due to their limited endurance and easy dielectric breakdown. These issues can be attributed to their large coercive field, which not only increases the operating voltage but also enhances the risk of dielectric breakdown. In this work, Ga-doped HfO_2 ferroelectric capacitors with varying concentrations and annealing temperatures are prepared by atomic layer deposition (ALD) technique for the first time, and their ferroelectric properties, crystal structure, polarization switching kinetics, and endurance characteristics have been systematically investigated. The results indicate that the Ga-doped HfO_2 ferroelectric films exhibit finely modulated coercive fields (E_c) ranging from 1.1 MV/cm (HfO_2/Ga_2O_3 = 32:1) to a very low 0.6 MV/cm (HfO_2/Ga_2O_3 = 11:1). Notably, under 650°C rapid thermal annealing, the W/Ga:HfO_2/W capacitors achieve a comprehensively good ferroelectricity, including a large remnant polarization ($2P_r$) of 32.0 μC/cm^2 and a small coercive electric field (E_c) of 0.8 MV/cm. Moreover, the capacitors exhibit robust breakdown reliability, including high breakdown electric field (E_{BD}, >4.5 MV/cm), large breakdown voltage (>2.7 V) for ten-year time-dependent dielectric breakdown (TDDB) lifetime, and surpassing endurance (>10^{10} cycles). The study introduces Ga doping as a viable strategy to enhance the reliability of HfO_2-based FeRAM.

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8:15am **AA1-TuM-2 Realizaton of Selector-Only Memory via Supercycle Atomic Layer Deposition of Ge-Sb-Se Ternary Alloy**, ***Jeongwoo Seo***, *Minu Cho, Inkyu Sohn,* Yonsei University, Korea*; Youngjae Kang, Jong-bong Park, Kiyeon Yang, Wooyoung Yang,* Samsung Advanced Institute of Technology, Republic of Korea*; Hyungjun Kim,* Yonsei University, Korea

In recent years, storage class memory (SCM) has been considered as a promising next-generation memory technology, combining fast data processing speed of dynamic random access memory (DRAM) with the non-volatility of NAND flash memory. Among SCMs, ovonic threshold switch (OTS) material-based selector-only memory (SOM) has emerged as a pivotal memory technique, presenting outstanding device performances in terms of power consumption, operational speed, and cycling endurance [1]. In addition, owing to the dual functionality (simultaneous memory and selector operation) of OTS material, its simple memory cell structure exhibits superior scalability, offering cost-effectiveness [2].

To meet the ever-increasing demands for lower fabrication cost and higher memory density, however, it is mandatory to devise vertical SOM based on three-dimensional vertical cross point (3DVXP) array structure. To fabricate vertical SOM devices, thin film deposition technique that guarantees conformal deposition of thin films on high aspect ratio structure is required. In this context, atomic layer deposition (ALD) is a promising thin film deposition technique for the realization of the vertical SOM devices.

In this study, Ge-Sb-Se ternary alloy was synthesized by supercycle ALD process using methanol as co-reactant to enhance the reactivity of precursors. ALD Ge-Sb-Se served as a dual functional material for the memory cell of SOM devices. The material properties of ALD Ge-Sb-Se were thoroughly investigated using various measurement tools. Controlling the sub-cycle ratio during supercycle ALD process, we were able to precisely control the chemical composition of Ge-Sb-Se ternary alloy and determine the optimal composition for the vertical SOM devices. Fabricated SOM devices exhibited average threshold voltage of 2.37 V and average memory window of 1.04 V. Our research results suggest ALD Ge-Sb-Se ternary alloy as an outstanding memory cell component for the next-generation vertical SOM technology.

Acknowledgement

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References

[1] Ravsher, Taras, et al. *IEEE Transactions on Electron Devices* 70.5 (2023): 2276-2281.

[2] Sung, Ha-Jun, et al. *Advanced Science* 11.44 (2024): 2408028.

8:30am **AA1-TuM-3 Atomic-Scale Thickness Control of Antiferroelectric ZrO_2 via Morphotropic Phase Boundary Engineering for Enhanced Ferroelectricity**, ***Chun-Ho Chuang***, *Ting-Yun Wang, Yu-Sen Jiang, Miin-Jang Chen,* Department of Materials Science and Engineering, National Taiwan University, Taiwan

This studydemonstrates the enhancement of dielectric and ferroelectric properties in sub-6 nm ZrO_2-based thin films by precisely modulating the atomic-scale thickness of the underlying HfO_2 seeding layer to engineer the morphotropic phase boundary (MPB) effect. By precisely tuning the seeding layer thickness to control the grain size and induce the in-plane tensile stress, the antiferroelectric (AFE, $P4_2/nmc$) to ferroelectric (FE, $Pca2_1$) phase transformation is triggered. Consequently, a high dielectric constant (ε_r ~ 38), low effective oxide thickness (EOT ~ 0.54 nm), and a high remanent polarization (P_r ~ 30 μC/cm^2) are achieved, while eliminating wake-up treatment and lowering the processing temperature to 400°C, which are highly favorable for integration with advanced semiconductor technology nodes. A novel application of helium ion beam microscopy (HIM) combined with Gwyddion software enables high-resolution imaging and quantitative analysis of nanoscale grain evolution during the AFE-MPB-FE transition. Compared to conventional scanning electron microscopy (SEM), HIM offers a sub-nm beam size, higher secondary electron yield, and minimal charging effects, enabling high-precision characterization of non-conductive ultrathin films without a heavy metal coating. This work overcomes critical scaling challenges — performance degradation in sub-6 nm FE films and high annealing temperatures — positioning ZrO_2 as a strong candidate for high-K dielectric layers and nonvolatile memory in AI, IoT, and neuromorphic computing.

8:45am **AA1-TuM-4 Metastable Rutile TiO2 Growth on Non-Lattice-Matched Substrates via a Sacrificial Layer Strategy**, ***Jihoon Jeon***, *Kim Seong Keun,* Korea Institute of Science and Technology (KIST), Republic of Korea

Metastable materials possess unique properties critical for advanced technologies; however, their synthesis is significantly challenging. Among the TiO_2 polymorphs, rutile TiO_2 stands out for its exceptional dielectric properties; however, its film growth typically requires high temperatures or lattice-matched substrates, limiting its practical applications. This article presents a novel sacrificial layer strategy for the atomic layer deposition (ALD) of pure-phase rutile TiO_2 films on diverse substrates, including amorphous Al_2O_3, HfO_2, and ZrO_2. This approach employs ultrathin Ru sacrificial layers to facilitate the formation of rutile TiO_2 seed layers via the in-situ generation of a rutile-matched RuO_2 lattice. At the same time, it is completely removed as volatile RuO_4 under exposure to O_3 during the ALD process. This approach eliminates the need for high-temperature annealing and substrate restrictions, enabling low-temperature formation of rutile TiO_2 on diverse substrates, including amorphous oxides. Comprehensive characterization revealed the structural stability of the films and their enhanced dielectric performance. Stabilizing rutile TiO_2 independently of the underlying layer opens new possibilities for its integration into memory capacitors. Furthermore, this strategy provides a versatile framework for stabilizing other metastable material phases, thereby offering opportunities for diverse applications.

9:00am **AA1-TuM-5 EWF Modulation and Electrical Performance Enhancement Using Fluorine Surface Treatment in Yttrium Oxide-based Dipole-First Gate Stack**, ***Sangkuk Han***, *Changhwan Choi, Wonjae Choi,* Hanyang University, Korea

Effective work function (EWF) tuning through dipole engineering is crucial for enabling multi-Vt options in advanced logic devices such as Gate-All-Around (GAA) nanosheets and Complementary-FET (CFET). The dipole-first approach is one of the most promising candidates for enabling multi-Vt engineering in next-generation logic devices. However, a primary challenge in this scheme is achieving precise Vt fine-tuning [1]. To address this, advanced shifter materials must provide fine-tunable EWF modulation to support diverse Vt flavors. In this study, Y_2O_3 was utilized as a dipole material to enable fine-tunable EWF modulation, while Fluorine Surface Treatment (FST) was applied to passivate defects in the high-k layer to improve electrical performance. Y_2O_3 exhibits strong resistance to fluorine-containing plasma, which prevents IL/channel degradation caused by fluorine plasma incorporation [2].

In this work, nMOS capacitors were fabricated to evaluate V_{FB} shift and electrical characteristics in dipole-first gate stack. By modulating the

thickness of ultra-thin lanthanide oxide films (La_2O_3, Y_2O_3) from 2 Å to 4 Å using atomic layer deposition (ALD). As shown in Fig. 1, V_{FB} reduction of pristine and fluorine-treated Y_2O_3 at 4 Å was observed at 200mV and 330mV, respectively. In contrast, La_2O_3 at 4 Å exhibited a large V_{FB} negative shift of 635mV, indicating a significantly broader tuning range. These results demonstrate that Y_2O_3 offers improved EWF fine-tunability, making it a more beneficial alternative to La_2O_3 in dipole-first gate stack. I-V characteristics show a consistent reduction with increasing thickness up to 4 Å for pristine Y_2O_3, whereas La_2O_3 exhibited a decrease only up to 3 Å, followed by an increase at 4 Å. This increase is attributed to IL regrowth and sub-oxide formation, potentially affecting the interfacial properties. Fluorine treated Y_2O_3 shows over an order of magnitude reduction in leakage current compared to pristine Y_2O_3 as shown Fig. 2. The improvement results from defect passivation within the high-k layer, particularly oxygen vacancies, while the strong resistance of Y_2O_3 to fluorine containing plasma helps prevent IL/channel degradation caused by fluorine incorporation.

Our results show that Y_2O_3 exhibits greater potential for fine-tuning compared to La_2O_3, while FST Y_2O_3 also showed improved electrical performance by maintaining a controlled negative V_{FB} shift with reduced leakage current. Our findings suggest that Y_2O_3 is a promising alternative dipole material for matching the threshold voltage requirements of next-generation advance logic devices such as a CFET architectures.

9:15am **AA1-TuM-6 ALD Young Investigator Award Finalist: Reconfigurable Memristor Crossbar for Graphlet Computing**, ***Kyung Seok Woo,*** Sandia National Laboratories*; Nestor Ghenzi,* Seoul National University*; Hyungjun Park,* Seoul National University, Republic of Korea*; A. Alec Talin,* Sandia National Laboratories*; Cheol Seong Hwang,* Seoul National University, Republic of Korea*; R. Stanley Williams, Suhas Kumar,* Sandia National Laboratories

In-memory computing approaches using memristor crossbars have been proposed as a paradigm shift to overcome the von Neumann bottleneck by combining memory and processing functions. Memristors are considered one of the most promising devices for in-memory computation due to their low power consumption, high switching speed, and scalability. However, sneak paths and stochastic behavior are two critical issues that limit their practical implementation. There have been transformative designs of in-memory computing using either stochasticity or sneak paths, but the combined potential of memristor crossbars remains unexplored. Here we propose a graphlet computing platform that synergistically utilizes both phenomena using a tunable hybrid memristor with a bilayer of insulator fabricated via plasma-enhanced atomic layer deposition (PEALD). By controlling the O_2 plasma power of PEALD, two oxide layers have different oxygen vacancy concentrations that allow for tunable switching behaviors under different switching conditions (Fig. 1). The tunable memristor was integrated into a crossbar, which was used to map a graph by assigning each device as either a node or an edge. Then, we performed graphlet computing by utilizing inherent sneak paths and stochastic behavior of the crossbar (Fig. 2). While the sneak paths are used to count graphlet structures for analyzing complex graphs, the stochasticity is implemented in a random walk process to efficiently solve computationally expensive problems. This newly proposed computing scheme demonstrates the advancement of memristor-based in-memory computing hardware by addressing the inherent issues of memristor technology.

9:30am **AA1-TuM-7 Tuning of Effective Work Function in Cl Free TiAlN ALD Through Fine Al Doping Process for Gate Electrode Application**, ***Gyeong Min Jeong,*** *Hae Dam Kim, Jin-Seong Park,* Hanyang University, Republic of Korea

In the advancement of semiconductor device fabrication, integrating high-κ dielectrics and metal electrodes is essential to overcome the limitations of traditional silicon-based MOSFETs. Titanium nitride (TiN) is a pivotal material, effectively mitigating diffusion-induced oxidation at polycrystalline silicon electrode interfaces. TiN have metallic properties like low resistivity and exceptional physical and chemical stability, render it indispensable in applications such as electrodes, surface coatings, and diffusion barriers. Work function of metal electrodes critically influences MOSFET electrical characteristics, including threshold voltage and leakage current. However, Fermi-level pinning in high-κ materials leads to deviations from intrinsic work function values, necessitating the consideration of effective work function values. For TiN, the effective work function typically ranges between 4.6 and 4.8 eV, aligning well with p-MOSFET. In contrast, n-MOSFET require lower work function values, prompting extensive research into methods for reducing TiN's work function to meet these requirements. Atomic layer deposition (ALD) has emerged as a cornerstone technique in semiconductor shrinking, offering unparalleled control over film thickness and composition. TiN thin films are commonly deposited via thermal ALD processes utilizing precursors such as titanium tetrachloride ($TiCl_4$) and ammonia (NH_3). This approach reliably yields high-quality films with low resistivity. However, the incorporation of chlorine residues necessitates post-deposition at temperatures exceeding 400 °C. Alternatively, metal-organic precursors like tetrakis(dimethylamido)titanium (TDMAT) can be employed; nevertheless, achieving low resistivity with TDMAT often requires plasma-enhanced processes or subsequent high-temperature annealing. In this study, we developed a thermal ALD process using TDMAT and NH_3 as precursors, incorporating trimethylaluminum (TMA) cycles to deposit TiAlCN thin films at a relatively low temperature of 300 °C. This method achieved films with a resistivity of approximately 5000 μΩ·cm, lower than previously reported values for thermal ALD TiN films deposited from TDMAT without post-deposition annealing. Furthermore, by doping aluminum concentrations below 10%, we successfully tuned the work function from 4.9 eV to 4.5 eV. Compared to conventional $TiCl_4$-based processes, our method offers advantages including reduced carbon contamination and lower deposition temperatures, thereby minimizing potential adverse effects on adjacent thin films. This makes the process particularly suitable for the fabrication of MOSFETs with increasingly complex architectures.

9:45am **AA1-TuM-8 Optimizing Grain Structure in Mo-Ru Alloys for High Conductivity**, *Changhwan Choi,* ***Hyunjin Lim,*** *Youngseo Na, Yeh Been Im,* Hanyang University, Korea

As the demand for continuous miniaturization in semiconductors increases, the search for new interconnect materials has become a key area of innovation. Conventional materials such as copper (Cu) face challenges related to increased resistivity, electron mobility limitations, and electromigration issues [1]. In addition, modern semiconductor processes impose stringent requirements on thermal stability, process compatibility, and interconnect reliability. Against this backdrop, molybdenum (Mo) and ruthenium (Ru) have emerged as promising candidates for next-generation interconnect materials [2]. Their high thermal stability, adaptability to ultrathin film deposition, and compatibility with advanced fabrication environments suggest the potential for a paradigm shift in interconnect design.

Mo and Ru have similar atomic radii, which minimizes lattice distortion when alloyed, thereby suppressing the increase in electrical resistivity [3]. Furthermore, the combination of Mo's superior oxidation resistance and Ru's ability to address barrier layer challenges enhances the reliability of interconnect structures. However, successfully integrating MoRu alloys into semiconductor interconnect technology requires reconsideration of nanoscale deposition techniques, including precise thickness control and uniform deposition on high-aspect-ratio structures. To address these challenges, plasma-enhanced atomic layer deposition (PE-ALD) plays a crucial role. Compared to conventional thermal ALD, PE-ALD provides additional reaction energy, enhancing surface reactivity and enabling deposition at lower temperatures, making it particularly suitable for back-end-of-line (BEOL) applications.

In this study, we employ PE-ALD to deposit MoRu thin films, investigating the control of alloy composition, grain growth mechanisms under plasma conditions, and the effect of plasma on film crystallinity. Furthermore, we evaluate the electrical resistivity of the films and conduct reliability tests under high-temperature annealing and current stress conditions. Mo films deposited by ALD exhibited a resistivity of 1167 μΩ·cm at 2 nm and 146 μΩ·cm at 8 nm, while Ru demonstrated an excellent resistivity of 20 μΩ·cm at 7 nm (Fig. 2). To investigate the size effect behavior, an MoRu alloy was fabricated and analyzed. By optimizing the deposition process and material properties, this study aims to assess the feasibility of MoRu as a viable alternative to Cu and W-based interconnects and provide fundamental data for its potential industrial implementation in future semiconductor manufacturing.

Author Index

Bold page numbers indicate presenter