ALD Applications
Room Tamna Hall BC - Session AA2-WeM

Display Applications

Moderators: Fan Yang, Huazhong University of Science and Technology, **Junjie Zhao**, Zhejiang University

8:00am **AA2-WeM-1 Remarkable Productivity and Performance of OLED Encapsulation through Growth Dynamics Control via Atmospheric Pressure Spatial Atomic Layer Deposition***, **Chi-Hoon Lee**, Kwang Su Yoo, Daejung Kim, Ji-Min Kim, Jin-Seong Park,* Hanyang University, Republic of Korea

The next-generation display industry is evolving beyond conventional liquid crystal displays (LCDs) by eliminating backlights and incorporating organic light-emitting diodes (OLEDs). These advancements have enabled applications in ultra-high-resolution displays for AR/VR, large-area displays, and stretchable/flexible displays. OLEDs commonly adopt low-temperature polycrystalline oxide (LTPO) pixel circuits, which utilize oxide semiconductors with low off-current as switching transistors and low-temperature polycrystalline silicon with high on-current as driving transistors.

Despite their advantages, OLED pixel circuits based on LTPO are susceptible to degradation when exposed to moisture, which can induce phenomena such as metal migration and delamination. Moreover, the infiltration of hydrogen into oxide semiconductors can cause a negative shift in threshold voltage, destabilizing the on/off states of thin-film transistors (TFTs). Therefore, high-performance encapsulation barriers are essential to protect OLED pixel circuits from moisture and hydrogen. Materials such as SiO_2, SiNx, and Al_2O_3 are under extensive investigation for this purpose. Among these, Al_2O_3 is well-known for its low water vapor transmission rate (WVTR) and low hydrogen permeability. Al_2O_3 films can be deposited using various methods, including evaporation, sputtering, plasma-enhanced chemical vapor deposition (PECVD), and atomic layer deposition (ALD).

ALD offers precise thickness control at the nanoscale and excellent conformality over high-aspect-ratio structures. However, conventional ALD processes, based on time-sequential operations, suffer from low deposition rates due to long purge times. Spatial ALD, which shortens the purge step duration, has been identified as a promising solution to overcome this limitation. However, the performance of spatial ALD requires careful optimization of parameters such as substrate speed and separation gas flow.

In this study, we investigated the growth behavior of Al_2O_3 films under various process conditions, focusing on the effects of substrate speed and trimethylaluminum (TMA) partial pressure. The growth behavior was analyzed based on the Langmuir adsorption model and expressed as the difference in growth per cycle (GPC). Four distinct process conditions, labeled A, B, C, and D, were evaluated. A hybrid process, combining the superior film quality of condition A with the high productivity of condition D, achieved exceptional performance metrics: a WVTR of 4.4×10^{-5} g/(m^2·day), hydrogen permeability of 1.7×10^{-4} barrer, and a deposition rate of 37.44 Å/min.

8:15am **AA2-WeM-2 Crystallinity Control through Composition Engineering for High-Performance $MgIn_xO_y$ TFTs via Thermal Atomic Layer Deposition***, **Ji-Su Bae**, Chi-Hoon Lee,* Hanyang University, Republic of Korea*; Sung-Hae Lee,* Entegris, Republic of Korea*; Jin-Seong Park,* Hanyang University, Republic of Korea

The next-generation display industry is continuously advancing into future technology domains such as AR/VR, free-form displays, large-area displays, and automotive displays. The next-generation display industry holds great promise for oxide semiconductors as new channel materials, owing to their low off-current and high mobility characteristics.Indium-based oxide semiconductors, characterized by high mobility due to their large 5s orbitals, require the introduction of carrier suppressor elements to effectively regulate high carrier concentrations. However, the suppression of charge concentration through the introduction of carrier suppressors is accompanied by a reduction in mobility. To address this issue, extensive research is being conducted on indium-based crystalline oxide semiconductors. The crystallization of indium-based oxide semiconductors has been reported through methods such as post annealing and the introduction of capping layers. This approach can also be extended from a material perspective, for instance, using Magnesium Indium Oxide ($MgIn_xO_y$).

$MgIn_xO_y$, a type of oxide semiconductor, is known to exhibit an inverse spinel crystal structure at a composition ratio of Mg:In = 1:2, which contributes to its high conductivity and enhanced doping efficiency due to the numerous interstitial sites [1]. $MgIn_xO_y$ can be deposited through various methods such as sputtering and spray pyrolysis [2, 3].However, the growth of $MgIn_xO_y$ utilizing ALD, which is renowned for its precise thickness and composition control in the next-generation display industry, has not yet been reported.

In this study, $MgIn_xO_y$with an indium composition range of from 43.3 to 77.0 at% were grown via thermal ALD with ozone as the reactant. It was confirmed that variations in the metal cation composition of $MgIn_xO_y$, controlled through the ALD process, influence the crystallinity of the thin films, which in turn affects the transfer characteristics of the fabricated thin-film transistors. The X-ray diffraction (XRD) analysis revealed the presence of a broad (311) diffraction peak in the $MgIn_xO_y$ thin films, which is associated with an inverse spinel crystal structure. The influence of the average grain size, calculated using the Debye-Scherrer relation for the corresponding plane, on the electrical performance of the TFTs was successfully demonstrated. Then, it is observed that the $MgIn_xO_{-y}$ TFTs with 65.5 at% of indium show excellent device characteristics (V_{th} = -0.1 V, μ_{FE} = ~15 cm^2/V s, S.S = 73.1 mV/dec) and reliability (ΔV_{th} = 0.89 V for PBTS condition).

8:30am **AA2-WeM-3 Nitrogen-Doped SiO_2 Gate Insulator for Enhanced Stability in ALD-IGZO TFTs***, **Tae-Heon Kim**, Dong-Gyu Kim, Jin-Seong Park,* Hanyang University, Republic of Korea

Silicon nitride (SiN_x) has gained attention as an insulating layer for oxide thin-film transistors (TFTs) due to its high dielectric constant and density, though its high hydrogen content can degrade device reliability. To address this, silicon oxynitride (SiO_xN_y) structures have been explored, leveraging the benefits of both SiO_2 and SiN_x through nitrogen incorporation. Among various doping techniques, atomic layer deposition (ALD) is particularly effective due to its low-temperature process, superior step coverage, and ability to minimize hydrogen-related bonds like Si–OH.

This study proposes a nitrogen doping strategy for SiO_2 gate insulators (GI) using a nitrous oxide (N_2O) plasma reactant to optimize the active layer/GI interface and bulk properties in top-gate bottom-contact (TG-BC) IGZO TFTs. Increasing N_2O plasma power from 100 to 300 W raised the nitrogen concentration in SiO_2 from 0.7 to 2.2 at% but also increased trap densities, leading to a U-shaped threshold voltage (V_{TH}) shift from -4.1 to 4.9 V under positive bias temperature stress (PBTS). Hydrogen annealing effectively reduced the V_{TH} shift from -2.1 to 0.0 V by chemically trapping hydrogen with nitrogen atoms. A hybrid GI structure using N_2O plasma at 150 and 300 W further improved PBTS stability and hydrogen resistance, highlighting the effectiveness of this approach in enhancing IGZO TFT reliability

8:45am **AA2-WeM-4 Engineering Hydrogen Content in SiN_X Thin Films via Precursor Control for Improved Oxide TFTs Characteristics***, **Sang-Hyun Kim**, Tae Heon Kim, Jin-Seong Park,* Hanyang University, Korea

Atomic layer deposition (ALD) has recently gained significant attention in the fabrication of high-performance display devices due to its self-limiting reaction mechanism, which enables atomic-scale thickness control and uniform thin-film deposition[1]. SiN_X gate insulators offer high dielectric constant and excellent encapsulation properties, enhancing Oxide TFTs performance. However, SiN_X films deposited by conventional CVD methods exhibit high hydrogen content, leading to reliability challenges in oxide TFTs[2]. Recently, ALD-based SiN_X has emerged as a promising solution due to its ability to deposit high-quality thin films compared to CVD, making it suitable for developing low-hydrogen SiN_X. ALD-based SiN_X can improve the mobility and reliability of oxide TFTs, positioning itself as a key material for next-generation high-performance displays.

This study compared TSA and DIPAS precursors to develop hydrogen-engineered SiN_X films for IGZO-TFTs. SiN_X was deposited with plasma power ranging from 100 W to 200 W. TSA exhibited over 3.8 times higher GPC than DIPAS at all power levels due to better chemisorption efficiency and minimal steric hindrance. Optimal films were achieved at 100 W for TSA and 150 W for DIPAS. TSA films showed higher refractive index, higher density, and 35% lower oxygen and 50% lower hydrogen content than DIPAS films. IGZO-TFTs were fabricated using SiN_X (20 nm) and SiN_X (15nm)/ SiO_2 (5 nm). TSA-SiNx-based devices demonstrated superior performance, with a V_{th} of -0.98 V, mobility of 61.8 cm^2/V·s, and zero V_{th} shift under PBTS, due to reduced hydrogen diffusion and trap density. In contrast, DIPAS-based devices exhibited poor V_{th} (-8 V) and reliability.

This study highlights the effectiveness of hydrogen-controlled SiN_X engineering in enhancing the mobility and reliability of IGZO-TFTs. These advancements meet the reliability and performance needs of next-generation displays.

References

1. Kim, Hye-Mi, et al. Atomic layer deposition for nanoscale oxide semiconductor thin film transistors: review and outlook. *International Journal of Extreme Manufacturing* 5.1 (2023): 012006.
2. Toda, Tatsuya, et al. Quantitative Analysis of the Effect of Hydrogen Diffusion from Silicon Oxide Etch-Stopper Layer into Amorphous In–Ga–Zn–O on Thin-Film Transistor *IEEE Transactions on Electron Devices* 61.11 (2014): 3762-3767.

9:00am **AA2-WeM-5 Remarkable Stability and Hydrogen Resistance on High-Mobility Oxide TFTs via N_2O Plasma Reactant in Atomic Layer Deposition**, ***So Young Lim***, *Sang-Hyun Kim, Yoon-Seo Kim, Taewon Hwang, Tae Heon Kim, Haklim Koo, Jin-Seong Park,* Hanyang University, Korea

Oxide semiconductor(OS) offers advantages for advanced applications such as high-performance Thin Film Transistors(TFT) and ultra-high-definition displays. Their high mobility, long-range uniformity, and extremely low off-current make them ideal for faster switching speeds, higher power efficiency. The application of ALD to OS fabrication has gained significant attention with reports of high field-effect mobility exceeding 50 $cm^2/V{\cdot}s$. Moreover, ALD provides precise controllability film thickness and composition to produce high-quality thin films. Despite the advancements, trade-off between field-effect mobility and device reliability remains a persistent challenge. Since OSs are highly sensitive to external influences, importance of GI becomes particularly pronounced in protecting them from external components like hydrogen. To mitigate these challenges, robust gate insulators(GIs) are pivotal in protecting OS active layers. Furthermore, researches are conducted to incorporate components to passivate defect sites in thin films.

This study explores N-doped Al_2O_3 as GI deposited by PEALD using N_2O reactant. The N content in the Al_2O_3 films increased linearly with plasma power (100–250 W), from 0.79% to 3.29%. 200W-deposited GI demonstrated a 3% improvement in hard breakdown voltage(7.81 MV/cm at 100 W to 8.08 MV/cm at 200 W) and 90% reduction in trap density compared to the 100W-deposited GI, resulting enhanced hysteresis properties. However, excessive plasma power at 250 W caused plasma damage and excess N content, degrading electrical properties. When applied to high-mobility TFTs, electrical properties were enhanced with increasing N_2O Plasma power. Optimized values include field-effect mobility of 53.45 cm^2/Vs, Vth of -0.03 V and SS of 67.7 mV/dec at 200 W plasma power. Moreover, the reliability under positive bias temperature stress(1h each under a gate electric field strength of 2 MV/cm and at 60℃) was also enhanced exhibiting slight negative Vth shifts of less than 0.18V. Incorporating N into Al2O3 has been demonstrated as an effective method to reduce bulk defects and suppress H diffusion, significantly enhancing device reliability. The hypothesis was validated by observing changes in field effect mobility and Vth value after 350℃ annealing in H-forming gas(H2 4% + N2 96%). This indicates suppressed H diffusion from the ambient into the active layer, thus demonstrating the H resistance of the Al2O3 dielectrics attributed to the increased N content in the GI layer.

Therefore, these findings highlight the potential of N-doped Al2O3 GIs deposited via optimized PEALD, to enhance the reliability and performance of oxide semiconductor-based devices.

9:15am **AA2-WeM-6 Highly Stable Fluorine-Anion Engineered ALD Indium Oxide Thin-Film Transistors towards BEOL Integration**, ***Jinxiong Li***, *Xinwei Wang,* School of Advanced Materials, Peking University, Shenzhen 518055, China

Back-end-of-line (BEOL) integration with oxide semiconductor thin-film transistors (TFTs) presents a highly promising approach for the continuation of the Moore's Law. To address the critical challenge of the oxygen vacancy (V_O) instability in high-mobility In_2O_3 TFTs, we propose a novel low-thermal-budget fabrication approach to realize fluorinated In_2O_3 (In_2O_3:F) TFTs with remarkable stability [1]. By combining a re-engineered ALD process for ultrathin In_2O_3 films with a novel plasma fluorination strategy, the afforded In_2O_3:F TFTs exhibited a high mobility (μ_{FE}) of 35.9 $cm^2/V{\cdot}s$, a positive threshold voltage (V_{th}) of 0.36 V, and small V_{th} shifts of 49 and −111 mV under positive and negative bias stress conditions, respectively. Density functional theory (DFT) analysis shows that the fluorine doping can stabilize the lattice oxygen and electrically passivate the V_O defects in In_2O_3 by forming the F_OF_i spectator defects. This work demonstrates a BEOL-compatible fabrication approach to achieve both high performance and high stability for the oxide TFTs, thereby highlighting their high promise for advanced BEOL integration.

[1] Jinxiong Li, et al., *Advanced Functional Materials*, 2024, 34 (28), 2401170

9:30am **AA2-WeM-7 High-Pressure Atomic Layer Deposition of Elemental Tellurium for Enhanced P-Type Semiconductors**, *Myung Mo Sung,* ***Dai Tran Cuong,*** Hanyang University, Korea

Tellurium (Te), with its unique helical structure, has emerged as a promising 2D p-type semiconductor. However, traditional deposition techniques face challenges in producing large-area, uniform Te thin films. Atomic Layer Deposition (ALD) offers a potential solution due to its capacity for high-quality, large-scale films. A primary obstacle in ALD-based Te deposition is insufficient nucleation at the initial growth stage, leading to island growth - a result of the low reactivity and bulky ligands of $(Me_3Si)_2Te$ and $Te(OEt)_4$ precursors. To address this, we introduce a novel approach that combines High-Pressure ALD (HP-ALD) with a Multiple-Dosing (MD) technique, promoting the formation of continuous, uniform Te films from the early stages of growth. The resulting Te thin films demonstrate a Hall mobility of 51.2 $cm^2\ V^{-1}\ s^{-1}$, strong stability, and excellent surface coverage. This advancement in Te thin-film fabrication through HP-ALD and MD addresses key challenges, paving the way for integrating Te into next-generation electronic devices.

9:45am **AA2-WeM-8 Ultrathin Sn-Doped in_2O_3 Films for Scalable Semiconductor Transistors**, ***Seung Ho Ryu,*** Korea University, Republic of Korea*; Taikyu Kim,* Korea Institute of Science and Technology (KIST), Republic of Korea*; Taeseok Kim, Seong Keun Kim,* Korea University, Republic of Korea

As transistor scaling progresses, ultrathin channel structures are increasingly required to suppress short-channel effects and enhance gate control in advanced device architectures such as FinFETs and gate-all-around (GAA) transistors. However, reducing channel thickness typically leads to severe degradation in conductivity, limiting the electrical performance of thin-film transistors (TFTs). In this study, we investigate an ultrathin Sn-doped In_2O_3 (ITO) channel to overcome this challenge. The uniform Sn doping enhances carrier density and mitigates the conductivity degradation associated with ultrathin channels, ensuring stable electrical performance. As a result, we successfully fabricate enhancement-mode TFTs with a 1.5 nm-thick ITO channel, achieving a high field-effect mobility of 33.4 ± 1.5 $cm^2/V{\cdot}s$, a subthreshold swing of 129 ± 30 mV/dec, and a threshold voltage of 0.3 V. These findings provide a crucial strategy for realizing high-performance oxide TFTs with ultrathin conducting channels, addressing a key challenge in the development of next-generation semiconductor devices.

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