ALD as the Solution for Uniform Cu Electroplating in High Aspect Ratio Vias

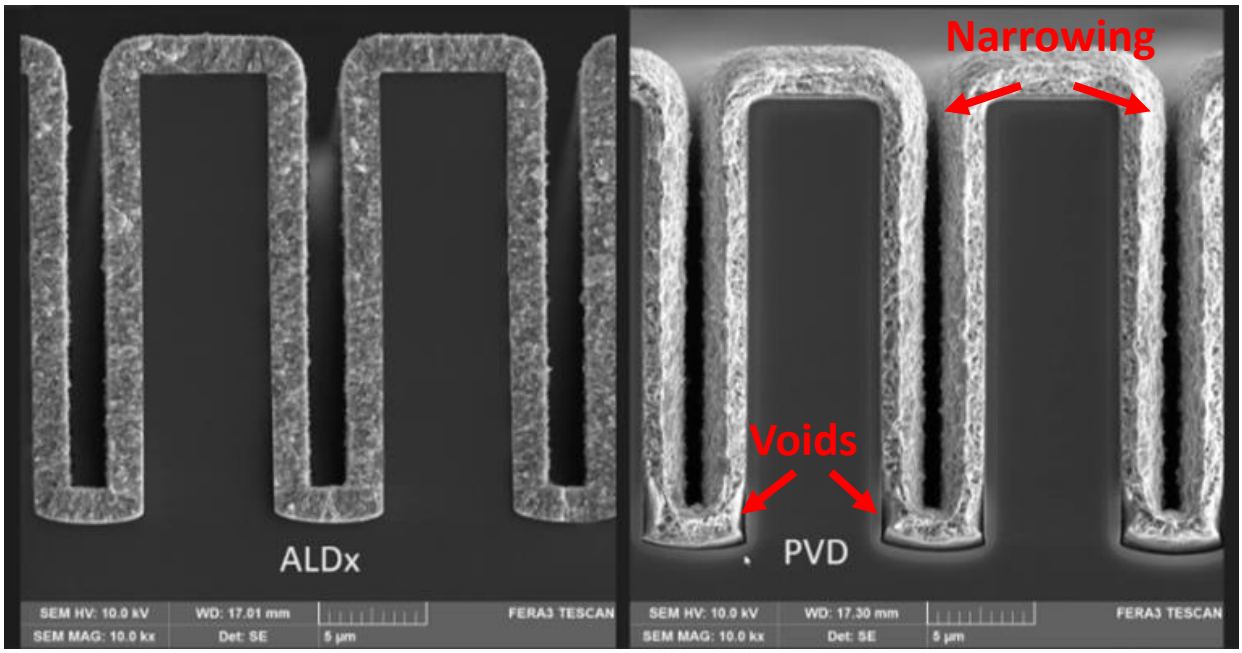

Figure 1: Scanning electron micrographs of thermal ALD SiO_2, TiN, Ru stack on the left and thermal oxide, PVD Ti/W, PVD Cu stack used for Cu electroplating. Notice on the left that the ALD stack is not visible on this scale, however the fact that Cu has been electroplated and remains well adhered are evidence of success. The image on the right shows two failure modes directly attributed to the PVD stack. First, electroplating has narrowing at the top, caused by a gradient in Cu seed, either higher thickness or lower resistivity at the top of the features. Second, voids at the bottom, likely caused by thin Cu adhesion (Ti/W) or seed layer resulting in delamination of Cu, thus creating a void and line failure.