ALD Applications
Room Ybor Salons I-IV - Session AA2-TuM
ALD Dielectric Applications

Moderators: Jiyeon Kim, LAM Research, **Olasehinde Owoseni**, Intel

10:45am **AA2-TuM-12 Sub-5 nm Indium Oxynitride Channel in Top-gated FETs Fabricated by PEALD for High-Performance 3D Transistor**, ***Doo San Kim***, *Minjong Lee, Soham Shirodkar,* The University of Texas at Dallas*; Min Gyeong Jo,* Hanyang University, Republic of Korea*; Thi Thu Huong Chu, Dushyant Narayan, Dan Le,* The University of Texas at Dallas*; Youngbae Ahn, Ja-Yong Kim, Seung Wook Ryu,* SK hynix, Republic of Korea*; Jiyoung Kim,* The University of Texas at Dallas

As silicon scaling approaches its physical limits, indium-based oxide semiconductors have emerged as promising channel materials because they maintain high carrier mobility and drive current even at channel thickness below 5 nm, enabling superior scalability. Among them, In_2O_3 exhibits excellent drive current; however, hydrogen incorporation leads to hydroxyl (OH) formation, resulting in device instability and threshold voltage shifts. Incorporating nitrogen to form indium oxynitride (InON) is expected to enhance mobility while effectively suppressing the formation of hydrogen induced OH bonds, thereby improving device stability.

Despite these advantages, direct deposition of InON via atomic layer deposition (ALD) is challenging because the bonding dissociation energy of In-O (~346 kJ/mol) is significantly stronger than that of In-N (~186 kJ/mol), making it difficult to incorporate sufficient nitrogen during the simultaneous supply of oxygen and nitrogen reactants.[1,2] In this work, we propose a two-step channel formation strategy: the initial deposition of an indium nitride (InN) thin film followed by an oxidation process to convert it into an InON channel layer.

In this presentation, we report the deposition of sub-5 nm conformal InN films via Hollow-Cathode Plasma (HCP)-enhanced ALD at 240 °C. To improve the structural and electrical stability of the channel, an annealing-based oxidation process was applied, converting InN into the more robust InON and evaluating their integration into top-gated (TG) thin-film transistor (TFT) devices. We investigated the influence of process parameters such as plasma power, process pressure, and deposition temperature for the film characteristics. The 5 nm InON layer was deposited at 240 °C, followed by the deposition of a 5 nm hafnium zirconium oxide (HZO) dielectric layer, and finally a TG-FET was demonstrated using Ni metal contacts. We presented InON TG-FET results, including transfer and output characteristics, temperature dependence, and channel length scaling. Our findings demonstrate that InON-based TFTs with a 100nm channel length achieve an on-current of ~1.2mA/μm at V_D = 1 V, an I_{on}/I_{off} ratio exceeding 10^9, and a contact resistivitywith Ni of 4 x 10^{-8} $\Omega{\cdot}cm^2$. In addition, the $\triangle V_{th}$ under positive and negative bias stress is 90 and 15 mV, at V_{ov} = ±1 V.

This work was supported by SK hynix Inc.

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[2] Luo, Y. R., "Bond Dissociation Energies" in CRC Handbook of Chemistry and Physics. (2010).

11:00am **AA2-TuM-13 V_{Fb} Control Technique of SiO_2/Dipole/$HfZrO_2$ Stack Structure Using New LaTiO and AlTiO Dipoles**, ***Tomomi Sawada***, *Toshihide Nabatame, Hiromi Miura, Manami Miyamoto, Takashi Onaya, Kazuhito Tsukagoshi, Naoki Fukata, Wipakorn Jevasuwan,* National Institute for Materials Science (NIMS), Japan*; Shinji Migita,* National Institute of Advanced Industrial Science and Technology (AIST), Japan

Dipole technique has been widely investigated to control the threshold voltage (V_{th}) of metal/High-k CMOS with GAA gate stack in 50 mV increments. La_2O_3 and Al_2O_3 are generally employed as n- and p-type dipoles. However, it remains a big issue of a large V_{th} shift in the sub-nm region of the dipole layer. In this paper, we investigated flatband voltage (V_{fb}) shift for SiO_2/dipole/$HfZrO_2$ stack structure using new LaTiO and AlTiO as n- and p-type dipoles.

p-Si/SiO_2/dipole/$HfZrO_2$/Au capacitor was fabricated at a maximum process temperature of 400 °C as follows: La_2O_3, TiO_2 and Al_2O_3 dipole layers were deposited on p-Si/SiO_2 (3.6 nm) by ALD at 250 °C with H_2O and La(iPrCp)$_3$, TDMAT, and TMA, respectively. LaTiO and AlTiO dipoles were also prepared by changing each ALD cycle of La_2O_3 and TiO_2, and Al_2O_3 and TiO_2 by ALD at 250 °C with H_2O, respectively. Next, an $HfZrO_2$ (2 nm) film was deposited on dipole layer by ALD at 250 °C using TEMA(Hf/Zr)(Hf/Zr = 1/1) cocktail and H_2O. Au gate electrode was deposited on $HfZrO_2$ film to form capacitor. Finally, forming gas annealing was carried out at 400 °C in 3%H_2.

The La_2O_3 and Al_2O_3 dipole capacitors exhibited negative and positive V_{fb} shifts as the La_2O_3 and Al_2O_3 dipole thickness increased, respectively. The V_{fb} shifts for the La_2O_3 and Al_2O_3 dipole capacitors were almost saturated, showing -0.35 and +0.32 V, respectively, when the dipole thickness was 0.8 nm. On the other hand, the TiO_2 dipole capacitor exhibited a V_{fb} shift of nearly 0 V regardless of the dipole thickness. This is due to differences in the strength and direction of the dipoles of La_2O_3, Al_2O_3 and TiO_2 at the SiO_2/dipole interface. The LaTiO (La = 0.46) dipole capacitors reduced the negative V_{fb} shift from -0.29 to -0.11 V compared to the La_2O_3 dipole capacitors when the dipole thickness was 0.2 nm. With a 0.2 nm thick dipole, the AlTiO (Al = 0.62) dipole capacitors also reduced the positive V_{fb} shift by approximately 25% compared to the Al_2O_3 dipole capacitors. This indicates that the dipole strength of La_2O_3 and Al_2O_3 can be effectively reduced by adding TiO_2 without dipole effect. In the LaTiO and AlTiO dipole capacitors, La and Ti atoms, and Al and Ti atoms, respectively, were piled up at the SiO_2/$HfZrO_2$ interface using STEM and EDS analysis. By employing new LaTiO and AlTiO dipoles in addition to La_2O_3 and Al_2O_3, V_{fb} controllability could be enhanced in the sub-nm region of the dipole layer. This is because TiO_2 without the dipole effect was added. This presentation is partially based on the results of the post-5G project (JPNP20017), entrusted to LSTC, commissioned by NEDO.

11:15am **AA2-TuM-14 Low-Temperature High-Pressure Deuterium Annealing for Defect Passivation in ALD-Deposited HfO_2 High-k Film**, ***Ji-Yeon Park***, *Seok-Won Lim, Gi-Beom Park, Chang-Kyun Park, Jin-Seong Park,* Hanyang University, Korea

Atomic layer deposition (ALD) is a key process technology for integrating high-k gate dielectrics into advanced semiconductor devices, providing excellent thickness control, compositional uniformity, and conformality. As conventional SiO_2 gate dielectrics reach their physical scaling limits due to increased direct tunneling leakage, high-k materials such as HfO_2 have been widely adopted [1]. Although ALD enables the formation of high-quality HfO_2 thin films, device performance is strongly influenced by defect states formed at the HfO_2/Si interface [2].In this study, ALD-deposited HfO_2 thin films grown using a Cp-Hf/O_3 process were investigated with a focus on the correlation between HfO_2/Si interfacial defect and electrical characteristics. Post-deposition deuterium treatment was employed not to modify the intrinsic quality of the ALD film, but as a post-ALD interface engineering and analytical tool to evaluate and improve defect states located at or near the interface. Electrical characterization using C–V and J–E measurements showed reductions in interface trap density, improved flat-band voltage stability, decreased leakage current density, and enhanced breakdown field after deuterium treatment, suggesting effective passivation of interface-related defects. Secondary ion mass spectrometry (SIMS) and X-ray photoelectron spectroscopy (XPS) analyses were conducted to examine deuterium incorporation behavior and changes in chemical bonding states, and their relationship to the observed electrical improvements was analyzed. These results indicate that the electrical performance of ALD-grown HfO_2 high-k dielectrics is governed primarily by interface quality rather than bulk film limitations. This work highlights the importance of post-ALD interface engineering and provides insight into ALD-compatible strategies for achieving reliable high-k/Si interfaces in next-generation semiconductor devices.Reference1) Wilk, Glen D., Robert M. Wallace, and JáM Anthony. "High-κ gate dielectrics: Current status and materials properties considerations." Journal of applied physics 89.10 (2001): 5243-5275. 2) E. P. Gusev,et al " Ultrathin high-k gate stacks for advanced CMOS devices," Microelectronic Engineering 69 (2003): 145-151.

11:30am **AA2-TuM-15 Infiltration of Porous SiOCH Thin Films by High-k Materials: Toward Nanocomposites with Enhanced Dielectric Properties**, ***Julie Chaussard***, *Stéphane Cadot, Marc Veillerot, Hélène Coudert-Alteirac, Nicolas Gauthier, Nicolas Bernier, Chloé Guérin, Aude Lefèvre,* CEA/LETI-University Grenoble Alpes, France*; Patrice Gonon,* Université Grenoble Alpes, CNRS, France*; Vincent Jousseaume,* CEA/LETI-University Grenoble Alpes, France

Dielectric materials, especially insulating polymers, are crucial for various technological applications due to their high breakdown voltage and low cost [1]. However, they generally exhibit low dielectric constant and thermal stability, limiting their use in field as power electronics.

To enhance their dielectric constant, recent studies have explored the elaboration of nanocomposites by adding alumina nanoparticles into a polymer matrix, resulting in significant improvements in dielectric constant and breakdown voltage even at low concentrations [2]. Despite these

promising results, the elaboration methods used were incompatible with standard microelectronic processes.

This work studies the elaboration of nanocomposite thin films using microelectronic materials stable up to 400°C, deposited by vacuum deposition techniques. To this end, 100 nm porous SiOCH were deposited by PE-CVD on Si wafers using a porogen approach [3]. Then high-k material was infiltrated into this porous thin film using ALD. The filling process for different materials and precursors was characterized using physicochemical methods (XRF, ellipsometry, XRR, ToF-SIMS, FTIR, TEM). Then, the electrical properties were studied (dielectric constant, dielectric losses, breakdown voltage). In the case of trimethylaluminum/O_3, the results highlight that the filling of the nanometric pores of the porous SiOCH occurs in the first ALD cycles (<5). Using an optimized recipe, a maximum filling of ≈50% of the porosity was obtained. As the number of cycles increases, high-k growth continues on the surface at a rate similar to that observed on Si. FTIR analysis reveals the formation of -OH groups in the first cycles, which increases dielectric constant and dielectric losses. A similar behavior is observed when using H_2O as oxidant. However, after 25 ALD cycles, the disappearance of -OH groups is observed for the TMA/O_3 process. One hypothesis is that the alumina layer formed on top of the porous structure becomes thick enough to limit H_2O adsorption into the matrix. This leads to the elaboration of composites with a dielectric constant 42% higher than that of the porous matrix while maintaining low dielectric losses. Finally, infiltration of porous SiOCH with HfO_2 and $HfZrO_2$ (from chlorinated precursors and water), which have higher dielectric constant than Al_2O_3, also enables enhanced dielectric properties without the presence of -OH groups. But in this case the filling rate is slightly lower than that observed with alumina.

In conclusion, this work demonstrates an easy approach for the elaboration of nanocomposites using standard microelectronic materials to achieve a broader range of electrical properties.

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[2] Zhang, T. et al.; *Sci. Adv.* **2020**, *6* (4), eaax6622.

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11:45am **AA2-TuM-16 Electrical Characterization of High-k ALD TiO_2 on AlGaN/GaN HEMT Structures**, ***Neeraj Nepal****, James G. Champlain, Vikrant J. Gokhale, Peter M Litwin, Brian P Downey, Virginia D Wheeler,* U.S. Naval Research Laboratory

Transport and breakdown field characteristics of GaN-based HEMT technologies are limited by high and non-uniform peak electric fields at the drain-edge of the gate. The non-uniform peak field causes premature electric field induced breakdown limiting the device performance [1]. These deleterious effects can be mitigated by integrating films with high dielectric constants (high-k, >20), such as TiO_2 [2-4]. For HEMTs, increased k leads to increased power handling capability without significant reduction in operation frequency. Thus, the goal is to integrate the highest k material possible. ALD provides flexibility in device design, integration and back-end-of line compatibility, making it a promising route for these high-k films. However, ALD high-k dielectrics with ideal interfaces and reduced trapping on AlGaN/GaN HEMTs have not been reported. In this talk, we report on the optimization and electrical characterization of the ALD TiO_2 interface with AlGaN-barrier HEMT structures.

Previously optimized deposition parameters [3] served as the baseline to further optimize electrical performance by pretreating the dielectric-barrier interface of $Al_{0.25}Ga_{0.75}N$/GaN HEMT structures. *Ex-situ* pretreatments including NH_4OH, UV O_3+BOE, piranha and O_2 plasma descum were studied. Similarly, *in-situ* UHV annealing, plasma treatments and their combinations were also studied. The optimum interface was found to be a combination of *ex-situ* O_2-plasma descum and *in-situ* H_2 and N_2 plasma treatments. Initial results using this preparation, a 20nm TiO_2 film demonstrated a reduction in gate leakage by 10^5 compared to a Schottky gate,zero CV hysteresis, a dielectric constant ≥ 50, and no significant change in 2DEG density. Even though the ALD TiO_2 has a narrower bandgap than AlGaN-barrier material, its large dielectric constant provides a pathway forward for dielectric permittivity engineering within the device structure. This engineering approach can improve breakdown voltage, lowers gate leakage and minimizes non-ideality over the state-of-the-art.

References:

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