Atomic Layer Etching
Room Tampa Bay Salons 3-4 - Session ALE-MoA
Plasma and/Energy-Enhanced ALE I

Moderators: Kyle Blakeney, Lam Research, **Heeyeop Chae**, Sungkyunkwan University (SKKU)

4:00pm **ALE-MoA-11 Atomic Layer Processing of Electronic Devices***,* ***Andreas Fischer****, Thorsten Lill,* Clarycon Nanotechnology Research, Inc.*; Fred Roozeboom,* University of Twente, Netherlands **INVITED**

Atomic Layer Etching (ALE) is increasingly adopted to meet atomic-scale patterning requirements in advanced semiconductor manufacturing. This work presents a comprehensive technical analysis of ALE fundamentals, process mechanisms, and performance metrics with emphasis on processing outcomes relevant to nanoscale and 3D device integration. ALE utilizes sequential, self-limiting surface reactions to achieve controlled etch-per-cycle behavior, enabling sub-nanometer material removal, excellent across-wafer uniformity, and reduced aspect-ratio dependent etching compared to reactive ion etching (RIE). Thermal and plasma-assisted ALE regimes are evaluated with respect to etch selectivity, damage mechanisms, and directionality. Thermal ALE demonstrates highly selective isotropic etching driven purely by surface chemistry, achieving minimal plasma-induced damage and enabling precise removal of oxides and high-k materials critical for advanced gate stacks and 3D architectures. Plasma-assisted ALE enables tunable anisotropy through low-energy ion activation while maintaining atomic-scale precision and improved surface smoothness relative to conventional plasma etching, supporting applications including contact hole formation, sidewall damage removal, and nanoscale pattern transfer. Process comparisons highlight ALE's superior uniformity, reduced excess-energy damage, and enhanced selectivity driven by self-limiting surface chemistry and controlled ion energies. Performance trade-offs—including throughput, precursor safety, chamber contamination, and temperature control—are analyzed to assess scalability toward high-volume manufacturing. The results demonstrate that ALE provides a robust pathway toward atomic-level etch control required for next-generation transistors, stacked memory devices, and heterogeneous material integration. Continued advances in precursor design, plasma control, and process optimization are expected to further expand ALE deployment in future semiconductor nodes.

4:30pm **ALE-MoA-13 Plasma-Enhanced Atomic Layer Etching of Mbe- and Ald-Grown Ultrathin HZO for Ferroelectric Tunnel Junctions***,* ***Marimuthu Rajendiran****, Nikolai Andrianov, Venkata Raveendra Nallagatla, Joaquín Miranda,* Silicon Austria Labs GmbH, Austria*; Polychronis Tsipas, Stavros Kitsios,* Institute of Nanoscience and Nanotechnology, National Center for Scientific Research "Demokritos", Greece*; Nathan Savoiad, Alexander Flasbyd,* Integrated Systems Laboratory, D-ITET, ETH Zurich, Switzerland*; Athanasios Dimoulas,* Institute of Nanoscience and Nanotechnology, National Center for Scientific Research "Demokritos", Greece*; Laura Bégon Loursd,* Integrated Systems Laboratory, D-ITET, ETH Zurich, Switzerland*; Deluca Marco,* Silicon Austria Labs GmbH, Austria

Abstract

Ferroelectric tunnel junctions (FTJs) based on $Hf_{0\cdot5}Zr_{0\cdot5}O_2$ (HZO) are promising candidates for next-generation non-volatile memory and neuromorphic computing owing to their CMOS compatibility, low power consumption, and fast switching speed. Scaling HZO to ultrathin dimensions (<4 nm) is critical to enhance FTJ performance in neuromorphic computing while maintaining robust ferroelectricity and energy efficiency. In this work, we present a systematic investigation of plasma-enhanced atomic layer etching (PE-ALE) of HZO thin films grown by molecular beam epitaxy (MBE), or by plasma-enhance atomic layer deposition (PEALD). The PEALE process employs a $Cl_2/BCl_3/Ar$ plasma chemistry at a substrate temperature of 50 °C, targeting controlled, layer-by-layer material removal. To support process development, density functional theory (DFT) and molecular dynamics (MD) simulations are used to establish a macroscopic fluid-dynamics-based framework for atomic layer etching, enabling identification of the energy window favorable for monolayer-scale removal of HZO. By tuning key process parameters such as RF power, plasma exposure time, and gas composition, an ALE window for HZO is identified. Furthermore, a comparative study between MBE- and ALD-grown HZO films highlights differences in etching behavior, including process window, surface morphology evolution, and implications for achieving ultrathin ferroelectric layers. These results provide important insights into thickness scaling strategies for ferroelectric HZO and offer a pathway to improve the FTJs device performance.

Reference

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4:45pm **ALE-MoA-14 Atomic Layer Etch Process for Nb and Ta Using CF_4/H_2 Plasma***,* ***Ryan Walsh****,* University of Nevada, Reno*; Mikeal B. Macera,* University of Nevado Reno, Carnegie Mellon University*; J. Russell Renzas,* University of Nevada Reno

Atomic layer etch (ALE) processes were developed for Nb and Ta on Si using a CF_4/H_2 plasma for the surface modification step and Ar^+ irradiation for the removal step. These materials are widely used in superconducting quantum device fabrication. The processes were investigated with respect to RF bias, CF_4/H_2 dose time, and Ar^+ etch time in order to identify the ALE window and saturation points. Ta and Nb yielded identical 0.23 +/- 0.01 nm/cycle etch rates for a soft-saturation process. The total cycle time was 16 sec with synergies of > 99% and 87% for Ta and Nb, respectively, and surface roughnesses were significantly reduced as compared to both the as-deposited films and an RIE process with similar chemistry. Over-saturated and under-saturated process were also investigated. A significant difference in EPC between different phases of Tantalum was also observed, suggesting crystal structure plays an important role in etch dynamics. Tantalum Nitride was also investigated due to its thin native oxide, which could help improve superconducting device performance.

To demonstrate the usability of these processes in industry, the effect of reduced purge times on ALE process performance was studied. For all processes the etch per cycle, selectivity, synergy, and surface roughness before and after were reported. A full process for Si was not studied but relevant parameters were reported. These processes are promising for real world manufacturing of devices that are sensitive to damage and require precise etch control.

5:00pm **ALE-MoA-15 Atomic-Precision Photoresist Line-edge Roughness Reduction via Plasma ALE***,* ***Richard Yang****,* Applied Angstrom Technology Pte. Ltd., Singapore

Line-edge roughness (LER) in photoresist patterns transfers through etch into final device features, directly impacting electrical variability and yield. Conventional plasma cure treatments reduce LER through bulk polymer reflow but lack independent control over material removal and do not address three-dimensional sidewall roughness. Here we demonstrate that plasma-enhanced atomic layer etching (PE-ALE) applied as a post-lithography treatment to 193 nm chemically amplified resist achieves LER reduction with atomic-scale precision alongside direct sidewall smoothing.

The process is cyclic atomic layer etching (ALE) with independently controlled modification and removal steps. A key finding is that the removal step bias voltage (Vpp) acts as a single control parameter switching between two distinct regimes: below threshold, etch-per-cycle approaches zero and the resist undergoes surface densification and crosslinking — evidenced by a 30% reduction in EPC for pre-hardened versus non-hardened resist. Above threshold, controlled material removal proceeds with PR thickness loss below 4%.

CDSEM measurements show LER (3σ) reduced by up to 30%, with a concurrent 17% decrease in correlation length indicating smoothing across the full spatial-frequency spectrum. Crucially, tilted-AFM sidewall line scans independently confirm surface roughness Rq reduction of 25%, providing orthogonal three-dimensional evidence that smoothing extends beyond the top surface to the resist sidewall — a contribution inaccessible to top-down metrology alone.

These results establish PE-ALE as a practical post-litho treatment capable of simultaneously reducing top-surface and sidewall roughness while preserving resist profile integrity, offering a new process handle for LER mitigation at advanced nodes. The ALE approach is much more controllable than the conventional RIE tool based plasma pre-treatment with independent control of modification and removal steps and angstrom level of removal of PR materials, which would be much needed for advanced logic and memory applications.

5:15pm **ALE-MoA-16 Comparative Study on Atomic Layer Etching Characteristics of Conventional C_4F_8 and Low-GWP C_3F_6**, ***Dong Ki Lee**, Chul-Hee Cho, Inho Seong, Dayeon Kang, Shinjae You,* Chungnam National University, Department of Physics, Republic of Korea

Atomic Layer Etching (ALE) has emerged as a critical technology for achieving atomic-scale precision in next-generation semiconductor fabrication. However, the high Global Warming Potential (GWP) of conventional perfluorocarbon gases widely used in the process, such as C_4F_8, necessitates the urgent development of eco-friendly alternative processes. In this study, we investigate the ALE characteristics of C_3F_6, a promising low-GWP candidate, in comparison with conventional C_4F_8 on silicon oxide (SiO_2) and silicon nitride (Si_3N_4) films to evaluate its feasibility for sustainable manufacturing, targeting high-selectivity applications such as the Self-Aligned Contact (SAC) process. The etching process was performed in an Inductively Coupled Plasma (ICP) reactor, where key parameters including bias power and step times were varied to verify the self-limiting behavior essential for ALE. We primarily focused on analyzing the process windows, etch rates, and etch selectivity derived from both C_4F_8 and C_3F_6 plasmas. Furthermore, to elucidate the reaction mechanisms and difference in dissociation pathways between the two gas systems, Residual Gas Analysis (RGA) was employed to analyze the gas-phase chemistry and monitor the evolution of neutral species and reaction by-products. In this presentation, we will discuss the potential of C_3F_6 to replace C_4F_8 by presenting the comparative analysis of process feasibility and investigating the correlation between plasma species and etch characteristics, thereby providing guidelines for eco-friendly semiconductor processing.

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