Atomic Layer Etching
Room Tampa Bay Salons 3-4 - Session ALE2-TuA

ALD+ALE and Selective ALE

Moderators: Jean-François de Marneffe, IMEC, **Austin Minnich**, Caltech

4:00pm **ALE2-TuA-11 Self-Limiting Oxidation State Control of MoOx Thin Films Using Integrated ALD and ALE**, ***Woojin Jeon***, *Chaeyeong Hwang,* Kyung Hee University, Republic of Korea*; Christophe Vallée,* University at Albany-SUNY **INVITED**

Atomic layer etching (ALE)has evolved beyond its intrinsic advantage of precise thickness controllability, and low-damage etching, with increasing research focused onadvanced process applicationssuch as the crystallization of ultrathin films as well as the realization ofgate-all-around (GAA)andthree-dimensional (3D) integrationstructures through integration withatomic layer deposition (ALD)andarea selective deposition (ASD).

In this talk, we present our research results oncontrolling the oxidation state of deposited thin films through the integration of ALD and ALE processes. Molybdenum dioxide (MoO_2) has attracted significant attention as a high-work-function electrode material for next-generation metal-insulator-metal (MIM) capacitors, particularly for stabilizing the rutile phase of TiO_2 with a dielectric constant of 150. However, typical ALD process only allows the most stable oxidation state of MoO3, resulting in stoichiometric variations in high-aspect-ratio structures and morphology degradation during reduction have limited its practical applications. To address these issues, we introduce an approach which combines ALD of MoO_a ($2 < a < 3$) followed by ALE of MoO_3 using H_2O. The process selectively removes MoO_3through etching, leveraging the self-limiting nature of both reactions to achieve precise atomic-scale control over oxidation states without morphology degradation. MoO_2 films deposited using this method exhibit enhanced electrical performance, including a higher dielectric constant and reduced leakage current when employed as bottom electrodes in TiO_2-base MIM capacitors.

4:30pm **ALE2-TuA-13 Selective Etching of Molybdenum and Tungsten Oxides Based on Their Oxidation States Using $SOCl_2$ and SO_2Cl_2**, ***Troy Colleran,*** University of Colorado at Boulder

Molybdenum, tungsten, and their oxides have important applications in microelectronics processing. This investigation explored the spontaneous etching of MoO2, MoO3, WO2, and WO3 by thionyl chloride (SOCl2) and sulfuryl chloride (SO2Cl2). The studies were conducted at 200°C using quadrupole mass spectrometry (QMS) and in situ Auger electron spectroscopy (AES). The QMS studies revealed selectivity between the +4 and +6 oxidation states of the metal oxides using SOCl2 and SO2Cl2 as the etchants. The in situ AES experiments demonstrated the removal of native oxide on both W and Mo thin films using SOCl2.

SOCl2 etched MoO3 and WO3 in the +6 oxidation state and produced MoO2Cl2 and WO2Cl2 and WOCl4, respectively. These volatile Mo and W oxychloride etching products were verified by QMS using their isotopic signatures (Figures 1 & 2). In contrast, SOCl2 did not etch the +4 oxidation state in MoO2. However, SOCl2 did etch WO2. SO2Cl2 displayed nearly opposite behavior. SO2Cl2 etched the +4 oxidation state in MoO2, but did not etch the +6 oxidation state in MoO3. SO2Cl2 also did not etch either WO2 or WO3. The lack of etching of WO2 by SO2Cl2 and the etching of WO2 by SOCl2 was attributed to the oxidation and disproportionation of WO2 to WO3.

In situ AES studies were used to evaluate the ability of SOCl2 to remove native oxide from Mo and W surfaces. After SOCl2 exposure at 250°C, the atomic percentage of oxygen on the metal films dropped from 59% on Mo and 53% on W before SOCl2 exposure to <2% on both films after SOCl2 exposure (Figures 3 and 4). SOCl2 has the potential to remove oxides on conductive Mo and W lines in BEOL interconnects. Oxidation and subsequent volatilization of the formed oxide also is a method for the thermal atomic layer etching (ALE) of Mo and W metals.

4:45pm **ALE2-TuA-14 High-Density Silicon Lines Patterning with Atomic Layer Etch Pitch Splitting (APS™) Technology**, ***Amin Karimi,*** *Robin Athle, Reza Jafari Jam, Alfred Ahlström Andersson, Svetlana Ivanova, Kishwar Sultana, Asif Muhammad, Mostafa Torbati, Hesamedin Safavi,* AlixLabs A.B., Sweden*; Fred Roozeboom,* University of Twente, Netherlands*; Dmitry Suyatin, Jonas Sundqvist,* AlixLabs A.B., Sweden

Dense silicon line fabrication is a central process in modern electronics manufacturing, enabling key device and interconnect structures such as FinFETs, gate-all-around FETs (GAA-FETs), gate electrodes, and metal interconnects.These features appear across multiple integrated-circuit layers, from front-end devices to back-end of line metallization layers (M0–M6), and are essential for logic and memory technologies. As device scaling continues, the ability to pattern denser line arrays with tighter pitch and smaller critical dimensions (CDs) has driven innovation. To meet scaling demands, advances in lithography and patterning have included deep ultra violet (DUV) immersion lithography, nanoimprint lithography (NIL), and low- and high-NA extreme ultraviolet (EUV) lithography. In parallel, multipatterning schemes such as SADP, SAQP, LELE, and SALELE have been developed to extend resolution limits. However, each approach has limitations. Immersion lithography faces fundamental resolution constraints, NIL suffers from defectivity and throughput challenges, and EUV adoption is hindered by very high capital and infrastructure and energy costs. Multipatterning further increases process complexity through repeated deposition, lithography, cleaning, and etching steps, leading to cumulative yield loss and stricter process control chalenges. As patterns reach a 24nm pitch and below, the high-aspect-ratio mandrils used to form silicon fins and nanosheets become prone to mechanical bending or collapse during the multiple deposition and etching cycles required by SAQP.

In this work, we present Atomic Layer Etch Pitch Splitting (APS™) patterning technology developed at AlixLabs[1-4] that simplifies dense line fabrication while extending the resolution of conventional lithography. The method is based on atomic layer etching (ALE) and serves as a more sustainable alternative to conventional multipatterning. It enables significant pitch reduction with a single processing step, reducing the need for EUV at certain technology nodes. In this way, patterns defined at 14/12 nm using immersion lithography can be scaled to effective dimensions corresponding to 7/6 nm and beyond, without EUV, lowering complexity and cost. The technique operates on patterns with arbitrary topology, including straight and inclined features, enabling orientation-independent line splitting. We demonstrate silicon dense line arrays with CDs of 10 nm and half-pitch of 10 nm. The process is repeatable, allowing multiple successive splitting steps equivalent to SAQP. Our single-step patterning process alternative, APS™, reduces yield variation and eliminates intermediate metrology needs.

1. Khan Md S. A., et al. US10930515 B2, Feb. 23, 2021, priority date March 14, 2017.

2. Khan Md S. A., et al. US11424130 B2, Aug. 23, 2022.

3. Khan Md S. A., et al., US20250259851 A1, Aug. 14, 2025.

4. Sundqvist J., et al. 13429, p. 134, SPIE, Apr. 22, 2025.

5:00pm **ALE2-TuA-15 Direct Atomic Layer Processing (DALP®): Extending ALD and ALE to Spatially Localized Multi-Material Integration**, ***Mira Baraket,*** ATLANT 3D Nanosystems, Denmark

The development of next-generation electronic and functional devices increasingly depends on the ability to integrate complex material heterostructures with nanoscale precision. However, conventional thin-film deposition and patterning workflows—while offering excellent uniformity and material quality—remain inherently rigid, limiting spatial selectivity, multi-material integration, three-dimensional thickness control, and rapid experimentation within a single process flow.

ATLANT 3D introduces **Direct Atomic Layer Processing (DALP®)**, a nanofabrication technology that enables digitally controlled, spatially localized deposition of multiple materials with atomic-scale precision. DALP combines the strengths of atomic layer deposition with direct-write spatial control, allowing different materials to be sequentially deposited at defined locations without intermediate lithography or masking steps. This capability enables the fabrication of complex material stacks, heterostructures, interfaces, and thickness gradients within a unified and repeatable workflow.

This presentation describes the DALP process architecture and its application across both combinatorial materials discovery and targeted device manufacturing. By enabling programmable material placement, precise thickness engineering, and high process repeatability within a single platform, DALP accelerates materials exploration while directly producing device-ready structures compatible with manufacturing environments. Representative examples demonstrate multi-material nanoscale structures for advanced semiconductor and functional material applications, where precise interface control, spatial selectivity, and scalability are critical.

DALP significantly expands the accessible design space for atomic-scale fabrication and provides a direct pathway from materials discovery to manufacturable, device-ready architectures.

5:15pm **ALE2-TuA-16 Atomic Layer Etching of Titanium Nitride with O_3 and $NbCl_5$**, ***Juha Ojala***, *Mykhailo Chundak, Anton Vihervaara, Mikko Ritala,* University of Helsinki, Finland

Titanium nitride is an essential material in the semiconductor industry, used as a gate metal and as electrode material in various devices, and as a diffusion barrier in metal interconnects. Future device architectures require materials to be formed into smaller and increasingly complex features, which drives the need for new deposition and etching processes. Thermal atomic layer etching, as an isotropic and conformal process is ideal for thinning and patterning films in high aspect ratio and non-line-of-sight structures. In some cases, ALE can also result in smoothing of the film surface, which could be used for interfacial engineering to improve device performance.

We present a new thermal atomic layer etching process for TiN based on oxidation of the TiN surface with O_3, and removal of the oxidized surface layer with $NbCl_5$. The process was studied at 200–350 °C and EPC values of 0.5–4.5 Å were observed. At 200–300 °C an Arrhenius type temperature dependence of the EPC was seen. Roughnesses of the films were studied using atomic force microscopy and it was found that at 200 °C the etching resulted in smoothing of the TiN surface from 0.7 to 0.6 nm RMS. The surface roughness was quite low even after etching at higher temperatures, as etching at 250–350 °C resulted in only slight roughening to about 0.9 nm RMS. Resistivities of the films were also measured, and it was found that the resistivity stayed comparable to the unetched film to a thickness of 4.5 nm. XPS measurements showed the presence of slight niobium oxide residue on the surface of partially etched TiN, but after full etching of the TiN film, no residues of the etchants could be seen.

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