Monday Morning, June 29, 2026

Plenary Session

Room HB Plant Ballroom - Session PS1-MoM

Plenary Session

Moderators: Parag Banerjee, University of Central Florida, **Virginia Wheeler**, U.S. Naval Research Laboratory

8:45am **PS1-MoM-1 ALD Welcome and Introductory Remarks***,*

9:00am **PS1-MoM-2 ALD Plenary Lecture: A Legacy of Atomic–Scale Innovation - Powering the AI Era***, Gurtej S. Sandhu,* Micron Technology **INVITED**

A commitment to innovation and creativity is required to meet demands of the new data age. These innovations help fuel the next generation of capabilities in Artificial Intelligence (AI) and enable technologies such as self-driving cars, smart medicine, industrial automation, space exploration etc. which sounded like science fiction not so long ago. The rapid rise of AI is reshaping computer architectures and placing unprecedented demands on memory performance and power efficiency. Memory has emerged as a critical enabler of modern AI systems, transforming memory from a supporting component into a central driver of system innovation.

This plenary talk explores how a legacy of atomic–scale process innovation has laid the foundation for today's AI memory era. Early adoption of atomic layer deposition (ALD) enabled key breakthroughs in memory scaling, establishing precision engineering as a strategic advantage that continues to scale with rising complexity. As chip complexity has been increasing exponentially, atomic–layer processes have become indispensable, enabling new device structures, tighter tolerances, and manufacturable solutions at extreme dimensions. In addition, there is need for advanced AI modeling tools to help engineers make informed decisions for building process flows faster, with less empirical experimentation. Traditional modeling however, has not kept up with pace and efficiency required for practical solutions and a unified approach across all facets of chip ecosystem and multi-disciplinary collaboration is needed. These solutions will require new breakthroughs in data processing and computational capabilities to enable more efficient and powerful multiscale modeling using advanced AI and physics-based approaches. By combining atomic–scale manufacturing with physics–based modeling and AI–driven insights, the industry is accelerating learning, reducing risk, and enabling faster innovation. Together, these capabilities are defining how memory will power the next era of AI.

Take–home message: *In the AI era, competitive advantage will belong to those who master atomic–scale manufacturing and amplify it with AI–driven technology development—turning complexity into speed, scale, and leadership.*

9:45am **PS1-MoM-5 ALD 2026 Innovator Awardee Talk: Atomic-Scale Engineering of Oxide Semiconductors by ALD: From Display Innovations to Semiconductor Channel Platforms***, Jin-Seong Park,* Hanyang University, Korea **INVITED**

Oxide semiconductors have transformed modern display backplanes by enabling high-performance thin-film transistors (TFTs) with low leakage current and low-temperature process compatibility. Yet extending oxide semiconductors from large-area electronics into semiconductor memory/logic introduces a new set of constraints—three-dimensional topography, stringent variability control, interface-limited transport, and integration-driven reliability requirements that are not easily met by conventional deposition schemes. Atomic layer deposition (ALD), with its self-limiting surface reactions, offers a unique pathway to address these challenges through conformal film growth on high-aspect-ratio structures and atomic-level control over thickness, composition, and interfaces.

In this plenary talk, I will present the evolution of my ALD research from display technologies—starting with OLED thin-film encapsulation and extending to oxide TFT channel/dielectric engineering—toward semiconductor channel applications based on ALD-grown oxide semiconductors. The discussion will focus on three practical "atomic-scale levers" that enable this transition. First, composition and stacking-sequence control in multi-cation oxides, using ALD super-cycles to tune carrier transport and uniformity. Second, crystallinity and defect management, where the balance between mobility and stability is engineered by controlling phase evolution and oxygen-related defects across nanometer-scale films. Third, interface and integration engineering—including dielectric/channel and contact interfaces, thermal budget considerations, and hydrogen-related reliability—aimed at compatibility with vertically integrated memory architectures.

Finally, I will outline a forward-looking roadmap in which atomic layer processes—combining ALD with selective interface modification and, where appropriate, atomic layer etching—provide manufacturable routes for oxide semiconductor channels in future 3D systems. By connecting display-validated ALD know-how to semiconductor integration demands, this talk will highlight how ALD oxide semiconductors can emerge as a scalable channel platform for the next era of vertically integrated electronics.

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