ALD Applications
Room Ybor Salons I-IV - Session AA2-WeM

ALD for Memory II
Moderators: Ji Hwan Ahn, POSTECH, **Andrea Illiberi**, ASM

10:45am **AA2-WeM-12 Upper-Layer-Induced Crystallization of Metastable Rutile TiO_2, *Jihoon Jeon,*** *Seung keun Kim,* Korea Institute of Science and Technology (KIST), Republic of Korea

The relentless scaling of dynamic random-access memory (DRAM) technology shrinks capacitor dimensions, thereby degrading charge retention time and triggering read instabilities. This drives the demand for high-permittivity dielectrics that surpass conventional HfO_2 or ZrO_2. Rutile TiO_2, with orientation-dependent permittivity ranging from 80 to 170, emerges as a compelling candidate. However, rutile TiO_2 is metastable under atomic layer deposition (ALD) conditions and requires elevated crystallization temperatures, which pose barriers to integration. Established ALD strategies stabilize rutile TiO_2 by employing lattice-matched bottom electrodes such as RuO_2, IrO_2, SnO_2, or MoO_2. Yet these approaches necessitate either replacing the bottom electrode or introducing additional rutile phase–inducing layers, thereby complicating compatibility with DRAM process flows. Moreover, the industry-standard TiN electrode, lacking lattice matching with rutile TiO_2, remains incompatible with such stabilization routes.

Here, we report for the first time the formation of crystal structure induced by an upper-layer during post-deposition crystallization. This upper-layer-driven templating effect provides a new pathway to control phase selectionin ALD-grown TiO_2thin films. After inducing rutile crystallization, the upper layer can be selectively removed without affecting the underlying structure, leaving a fully crystallized rutile TiO_2. This strategy enables the integration of high-k rutile TiO_2 while preserving the TiN bottom electrode, thereby ensuring full compatibility with DRAM fabrication processes

11:00am **AA2-WeM-13 Surface-Reaction-Energetics-Driven Stabilization of Rutile TiO_2 at Low Temperatures in Atomic Layer Deposition, *Seungwan Ye,*** *Jihoon Jeon, Jongseo Kim, Seong Keun Kim,* Korea Institute of Science and Technology (KIST), Republic of Korea

As the physical dimensions of dynamic random-access memory (DRAM) continue to scale down, maintaining sufficient charge capacitance has emerged as a key challenge for next-generation memory technology. Therefore, to overcome the limitations of current Zr-based dielectrics, high-k materials with a higher dielectric constant are essential. Among them, rutile TiO_2 is the most promising dielectric due to its high dielectric constant ($k > 80$).

However, the rutile phase of TiO_2 is thermodynamically metastable, typically requiring high temperature process above 600℃, which exceeds the thermal budget for the DRAM fabrication process. Although using lattice-matched rutile bottom electrodes such as RuO_2, IrO_2 and MoO_2 has been proposed to form rutile TiO_2 at low temperatures, their poor process compatibility with the industry-standard TiN bottom electrode remains a critical obstacle.

In this study, we propose a novel method using surface reaction during ALD that enables the growth of metastable rutile TiO_2 thin films at a low temperature of approximately 330°C, irrespective of the bottom electrode. This breakthrough allows for the successful deposition of high-quality rutile TiO_2 on various substrates, including the industry-standard TiN, thereby dramatically enhancing its commercialization potential for next-generation memory devices.

11:15am **AA2-WeM-14 Magnetism of Ultrathin TiO_2 Films Prepared by Atomic Layer Deposition, *Jhonatan Rodriguez Pereira,*** *Jan Macak,* University of Pardubice, Czechia

Semiconducting oxides are gaining attention for spintronic applications due to their tunable electronic and magnetic properties.[1,2] Among them, TiO_2 is a widely studied semiconducting oxide for a wide range of applications owing to its chemical stability, wide band gap and versatile functionality.[3-5] The observation of room-temperature ferromagnetism in undoped TiO_2 films has raised fundamental questions regarding its origin, which has been frequently linked to intrinsic defects, reduced dimensionality, and interface effects rather than conventional magnetic doping.[6-8] Several studies addressing this phenomenon have focused on films prepared by pulsed laser deposition.[9-11] Given the strong sensitivity of defect-induced magnetism to film thickness and interface quality, a deposition method enabling atomic-scale control is particularly desirable.

Atomic Layer Deposition (ALD) provides an ideal platform to address this necessity, owing to its precise control over thickness and composition, as well as its ability to produce smooth and conformal ultrathin films.

In our recent paper, [12] we showed for the first time the ALD growth of ultrathin TiO_2 films (below 10 nm) on $LaAlO_3$ substrates. Structural characterization confirmed the formation of anatase TiO_2 films. Magnetic measurements revealed a pronounced thickness-dependent behavior, with ferromagnetic responses observed for films of intermediate thickness, while thinner films remained diamagnetic. The magnetic signal was strongly anisotropic and confined to the film plane, suggesting a two-dimensional origin associated with surface and interface effects. Complementary chemical and computational analysis indicate the presence of oxygen-related defects, whose concentration varies with film thickness.[12]

The presentation will introduce and describe the ALD growth of ultrathin TiO_2 films, together with their structural, chemical, magnetic, and theoretical characterization, and will discuss the role of defects and interfaces in the emergence of ferromagnetism.

References:

[1] Hang, Y. et al. Front. Mater. 11 (2024) 1444769. [2] Singh, S. et al. Opt. Quant. Electron. 55, (2023) 123. [3] Gualdron-Reyes, A. F. et al. New J. Chem. 42 (2018) 14481. [4] Martinez, H. et al. J. Mol. Catal. A: Chem. 423 (2016) 248. [5] Carreno-Lizcano, M. I. et al. Catal. Today 341 (2020) 96. [6] Wei, X. et al. J. Appl. Physics 105, (2009) 07C517. [7] Wang, H. et al. J. Appl. Physics 115, (2014) 233909. [8] Zhang, Y. et al. J. Magn. Magn. Matter. 443, (2017) 202. [9] Hong, N.H. et al. Phys. Rev. B: Condens. Matter Mater. Phys. 73, (2006) 104. [10] Yoon, S. et al. J. Phys.: Condens. Matter 18, (2006) L355. [11] Quynh Nhu, T.et al. J. Phys. D Appl. Phys. 57, (2024) 265302. [12] Rodriguez-Pereira, J. et al. ACS Appl. Nano Mater. 8 (2025) 20105.

11:30am **AA2-WeM-15 Low-Temperature Peald of Silicon Nitride Using Diiodosilane for High-Conformality Spacers of Three-Dimensional Memory Devices, *Jiabao Sun,*** *Tielu Liu, Xin Zhang, Gang Song, Hongbo Sun, Baodong Han, Chao Tian, Chao Zhao,* Beijing Superstring Academy of Memory Technology, China

Silicon nitride (SiN_x) thin films are critical insulating spacers for next-generation high-density memory devices[1]. Transitioning to extreme 3D stacking with deep lateral pockets imposes rigorous demands on plasma-enhanced atomic layer deposition (PEALD)[2]. Specifically, maintaining high-quality films at low thermal budgets is vital for integration with temperature-sensitive amorphous oxide channels. In this work, we investigate a low-temperature PEALD SiNx process using Diiodosilane (DIS, SiH_2I_2). The selection of DIS is motivated by the low dissociation energy of the Si-I bond (~284 kJ/mol)[3], which facilitates efficient precursor activation and surface reactions at reduced temperatures compared to chlorinated or aminated silanes.

We report a comprehensive optimization to address two critical research questions: the achievement of high lateral conformality and the spatial uniformity of the wet etch rate (WER) across complex 3D geometries. A significant reduction in the WER (30:1 HF) of the SiN_x films is achieved, dropping from ~120 nm/min to ~3 nm/min via precise plasma chemistry modulation (Fig. 1). A strong positive correlation between WER and growth per cycle (GPC) indicates that high-growth regimes are associated with plasma-induced damage and reduced film density. X-ray Photoelectron Spectroscopy (XPS) analysis revealed that high WER correlates with a shift in nitrogen bonding environments, specifically the presence of sub-stoichiometric NSi_2O and $NSiO_2$ species over the preferred NSi_3 configuration (Fig. 2). Furthermore, a distinct I peak is identified in high-WER samples, indicating that unreacted precursor fragments at high radiofrequency (RF) power and H_2 flow rates degrade the structural integrity of the film.

To address 3D integration challenges, we achieved ~94% lateral conformality within high-aspect-ratio structures (Fig. 3). Reducing the process pressure from 22.5 Torr to 4 Torr increases the molecular mean free path, enhancing precursor diffusion into deep features. Additionally, minimizing RF power reduces ion directivity, promoting the conformal profile essential for lateral coverage. Notably, the WER within the confined side-pockets was reduced by approximately one order of magnitude, achieving exceptional spatial uniformity across the 3D architecture (Fig. 4). These optimizations provide a robust process window for subsequent Wet etch or Certas gas etching, ensuring structural integrity in 3D integration.

This study provides a viable pathway for high-quality SiN_x spacers in temperature-sensitive 3D memory architectures.

Reference

1. F.M. Cunha, et al., Mater. Sci. Semicond. Process. 2026.2. V. Cremers, et al., Appl. Phys. Rev.2019.3. H.B. Profijt, et al., J. Vac. Sci. Technol. A Vacuum, Surfaces, Film. 2011.

11:45am **AA2-WeM-16 A Nanolaminate Cushion Approach for Stabilizing Ultrathin Al_2O_3 and SiO_2 Dielectrics in Future Logic and Memory Technologies**, *Mahesh Nepal, Tanka Bhushal,* ***Tara Dhakal,*** Binghamton University

Continued scaling of DRAM capacitor dielectrics and emerging memory devices requires ultrathin insulating layers that maintain low leakage and high reliability. Comparable challenges are also present in embedded and BEOL decoupling capacitors, where capacitance density and electrical stability are critical. However, once oxide dielectrics reach the few-nanometer regime, leakage increases dramatically and breakdown margins collapse, making dielectric reliability a primary limiter to further scaling. Here, we present a novel dielectric stabilization strategy using an atomic layer deposited (ALD) Al_2O_3/TiO_2 nanolaminate engineered to function as a controlled conductive “cushion” interlayer that enables reliable scaling of ultrathin dielectric films.

Spectroscopic analysis using hard X-ray photoelectron spectroscopy indicates oxygen-deficient TiO_2 and compositionally modified Al_2O_3 networks, producing a quasi-conductive nanolaminate that suppresses catastrophic dielectric failure. Electrical impedance measurements confirm that while the nanolaminate exhibits non-ideal dielectric characteristics independently, integration with ultrathin capping dielectrics restores stable capacitive behavior.

Using planar metal–insulator–metal capacitor test structures, we demonstrate that an optimized nanolaminate period enables scaling of Al_2O_3 dielectrics to ~3 nm while achieving leakage current densities near 10^{-7} A/cm^2 at 1 V and capacitance densities approaching 20 fF/um^2 across large-area devices. The stabilization approach is further shown to be transferable to SiO_2-based dielectric stacks, indicating broader material compatibility.

From a memory-scaling perspective, modeling suggests that integration with three-dimensional capacitor geometries could significantly amplify capacitance density, positioning this cushion-enabled architecture as a promising pathway for next-generation DRAM applications. More broadly, this work demonstrates how intentionally engineered leaky nanolaminates can serve as functional interfacial layers to overcome reliability bottlenecks in aggressively scaled dielectric stacks.

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