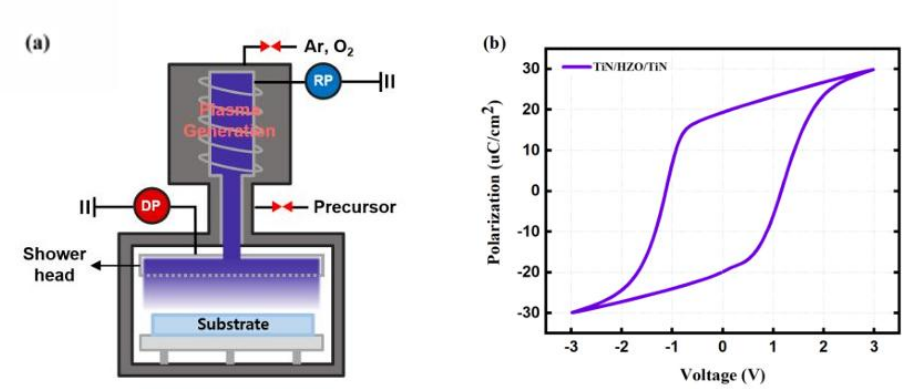

Fig. 1. (a) Schematic diagram of the CP-ALD system, (b) Polarization-electric field (P-E) hysteresis loops of the ferroelectric thin film.

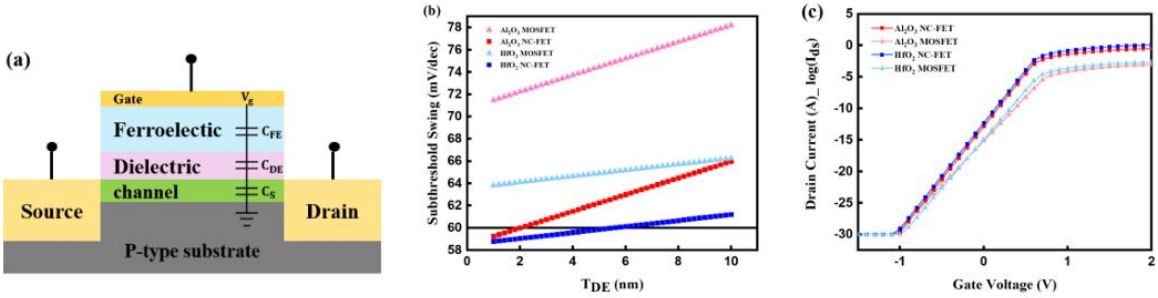

Fig. 2. (a) Schematic of the NC-FET device structure used for modeling, (b) Modeled SS values of NC-FET and MOSFET as a function of dielectric layer thickness, and (c) Comparison of transfer characteristics between the optimized NC-FET and conventional MOSFET.