**Leveraging Topographic Etch Selectivity: Atomic Layer Etch Pitch Splitting (APS™)**

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As the semiconductor industry pushes beyond sub-20-nm feature sizes, the limitations of traditional multiple patterning techniques, such as Self-Aligned Double/Quadruple Patterning (SADP/SAQP) and Litho-Etch-Litho-Etch (LELE), become increasingly apparent. These methods rely on complex, multi-step cycles of deposition, lithography, and etching, which escalate costs, increase variability, and significantly increase environmental impact. Atomic Layer Etch Pitch Splitting (APS™) technology enables multiple patterning by utilizing the topographic selectivity of Atomic Layer Etching (ALE).[1-4] This topographic selectivity transforms nanostructure sidewalls into etch masks, eliminating the need for spacer layer deposition. As a result, APS™ provides a more affordable and sustainable alternative to achieve pitch multiplication with high precision.

In this work, we demonstrate the versatility of APS™ across two critical integration paths: high-density scaling by a repeated application of the APS™ process and the APS™ process integration with different lithographic techniques. The process integrates seamlessly into existing industrial workflows, enabling the selective removal of material from the center of pre-patterned features, Figure 1a. We show that initial features with critical dimensions (CDs) below 100 nm can be split without additional lithography steps or sacrificial spacer layers, achieving results comparable to state-of-the-art patterning techniques. As an example, Figure 1b illustrates a representative Si line pattern obtained after applying APS™ to Si lines produced using standard immersion ArF lithography (ArFi). The resulting structures featuring CDs of 10 nm, a half-pitch (HP) of 12.5 nm, and a line width roughness (LWR) of 2.2 nm demonstrate that APS™ enables features comparable to those achieved by leading-edge lithographic and patterning methods such as immersion ArF lithography (ArFi), Extreme Ultraviolet lithography (EUVL), and Nanoimprint lithography (NIL). At the same time, the reduced process complexity of APS™ directly translates into lower capital expenditures (CAPEX) and operating costs (OPEX), higher throughput, and reduced $CO_2$-equivalent emissions. These advantages position APS™ as a sustainable and scalable solution for next-generation logic and memory devices, offering a pathway to advanced resolution that bypasses the complexity and high costs of traditional multi-patterning.

*References:*

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2. Khan Md S. A., et al. US11424130 B2, Aug. 23, 2022.
3. Khan Md S. A., et al., US20250259851 A1, Aug. 14, 2025.
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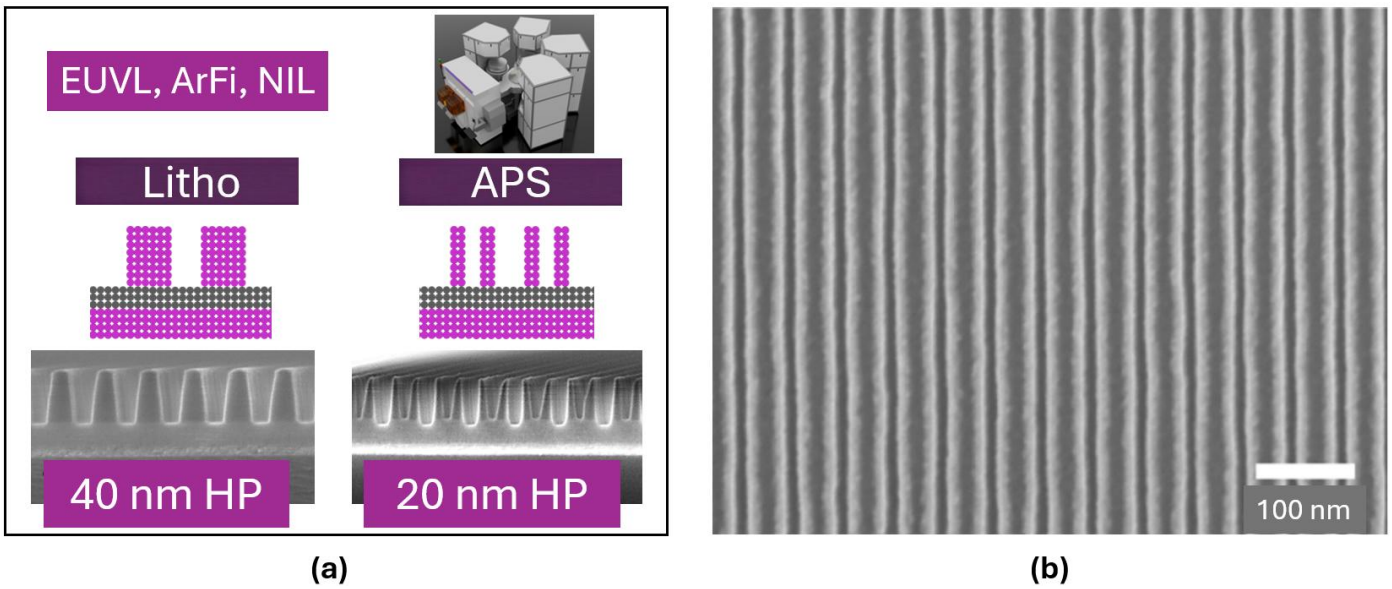


**Figure 1.** Pushing technology boundaries: (a) APS™ reducing pitch splitting to a single-step process with higher throughput, lowering environmental impact, and scalability potential beyond sub-2 nm technology nodes. (b) Representative Si line pattern with an original half-pitch (HP) of 25 nm after a single APS™ process step. The resulting structures exhibit a critical dimension (CD) of 10 nm, an HP of 12.5 nm, and a typical line width roughness (LWR) of 2.2 nm. The original Si lines were produced using standard immersion ArF lithography (ArFi).