Tuesday Afternoon, October 22, 2019

Plasma Science and Technology Division Room B131 - Session PS+EM-TuA

Advanced BEOL/Interconnect Etching and Advanced Memory and Patterning

Moderators: Hisataka Hayashi, Toshiba, Japan, Kenji Maeda, Hitachi High Technologies America Inc.

2:20pm PS+EM-TuA-1 BEOL Etch Challenges and Solutions for Advanced Process Nodes, Angélique Raley, K Lutker-Lee, X Sun, Y Lu, Q Lou, N Joy, M Edley, TEL Technology Center, America, LLC; K Taniguchi, M Honda, TEL Miyagi Limited, Japan; P Biolsi, TEL Technology Center, America, LLC INVITED

As logic nodes continue to scale below 7 nm, the back-end-of-line (BEOL) critical pitch has moved to sub-40 nm and is forecasted to scale down to 14 nm according to the latest International Roadmap for Devices and System (IRDS). This aggressive scaling has led to an industry wide effort in terms of materials research to manage interconnect resistance, patterning innovations to control for process variation impact and an increased focus on self-limited or highly selective processes.

In addition to the patterning and integration complexities that arise with scaling, pitch reduction has a direct impact on the plasma etch-processing window. Conventional continuous wave processes can no longer achieve stringent aspect ratio dependent etching (ARDE), selectivity and profile control requirements and have gradually given way to pulsed plasma processes, decoupled process sequence plasmas or remote plasmas to widen the process space.

In this talk, we will give an overview of plasma etching challenges and solutions for the BEOL in terms of patterning integration, dielectric etch and new materials introduction.

3:00pm PS+EM-TuA-3 Enabling Fully Aligned Via for Advanced BEOL Nodes Scaling -Etch and Film Co-optimization, *Xinghua Sun*, *A Raley*, TEL Technology Center, America, LLC; *J Lee*, *J Arnold*, IBM Research Division, Albany, NY; *K Taniguchi*, TEL Miyagi Limited, Japan; *M Edley*, *K Lutker-Lee*, TEL Technology Center, America, LLC; *D O'Meara*, Tokyo Electron America, Inc.; *K Tapily*, *Y Lu*, *P Biolsi*, TEL Technology Center, America, LLC

Aggressive metal pitch scaling of back end of line (BEOL) interconnect for future nodes leads to increased sensitivity to via overlay and critical dimension (CD) errors, resulting in yield loss. Spacing between top and bottom metal layers in via chain macros are reaching the limits of current materials, such that device reliability may become compromised due to metal shorting or dielectric breakdown. The technique of 1-D self-aligned via (SAV) constrained by top metal hard mask (MHM) is widely used to control one direction of via CD. 2-D fully aligned via (FAV) was recently introduced to mitigate the drawbacks of SAV at via bottom. In FAV, vias are constrained with spacers resulting from recessed metal in the orthogonal direction to the MHM, thereby increasing the margin of error allowed due to CD variations and overlay shifts. However, one of the biggest challenges in successfully integration of FAV in the BEOL is maintaining the integrity of these spacers during via etch. Etch selectivity, landing on conformably deposited Nblok based cap layers, is far from sufficient to maintain good self-confinement that demonstrates adequate FAV behavior. High selectivity etch stop layers (ESL) along with compatible etches that promote soft landing on these films are required.

In this presentation, we demonstrate that etch and film can collaboratively work to make FAV a competitive solution for sub-7nm nodes. Different ESL materials and film properties are investigated in conjunction with unique via and trench etch processes to achieve optimized FAV corner shape. This work shows a multifaceted approach to successful implementation of FAV as a valuable scaling booster for advanced BEOL nodes.

3:20pm PS+EM-TuA-4 Non-selective Silicon Oxide and Nitride Etch in Oxygen/Nitrogen-containing Fluorocarbon Plasmas, Yu-Hao Tsai, D Zhang, Y Han, J Baillargeon, Y Shi, H Kim, M Wang, TEL Technology Center, America, LLC; T Yokoyama, M Iwata, Y Kihara, M Honda, W Sakamoto, Tokyo Electron Miyagi Ltd., Japan; A Mosden, A Metz, P Biolsi, TEL Technology Center, America, LLC

Performing an all-in-one etch process for 3D-NAND fabrication requires comparable and high etch rates (E/R) for SiO₂ and Si₃N₄; the goal remains challenging. As the discrepancy of E/R largely results from the different nature of materials, surface modifications of SiO₂ and Si₃N₄ to achieve comparable composition during etch can improve the desired non-

selectivity. In the presented work, we study the conversion of SiO₂ [Submitted] and Si₃N₄ [J. Micro. Manuf.1, 20180102 (2018)] to oxynitride (SiO_xN_y) via the nitridation and oxidation-etch reactions, respectively. We computationally identify the etching mechanism of SiO₂/Si₃N₄ in the N/Ocontaining fluorocarbon plasmas using both quantum chemistry (QC) and molecule dynamics (MD) simulations; the surface conversion to SiO_xN_y is predicted. The results are further validated by the plasma etching of blanket SiO₂ and Si₃N₄ films in a Capacitively Coupled Plasma (CCP) chamber; both E/R trends and surface analysis on validation of oxinitride and/or nitrioxide (SiO_xN_y) formation using methods such as XPS, EDS etc. are discussed. We detail the etch reaction pathway, in which the elimination of O/N atom forming nitric oxide (NO) species is predicted. Along with that, the synergy of having F species in the process is justified. Finally, we discuss the impact of fluorocarbon to N/O ratio on the preference of either high E/R or active SiO_xN_y formation. The research builds a foundation for future development work on pursuing robust all-inone non-selective SiO₂/Si₃N₄ etch processes.

4:20pm PS+EM-TuA-7 Challenges in High-aspect-ratio Hole Etching for 3D Flash Memory, Mitsuhiro Omura, J Hashimoto, T Adachi, Y Kondo, M Ishikawa, J Abe, I Sakai, H Hayashi, Toshiba Memory Corporation, Japan INVITED

Memory devices with higher bit density are required for effective use of big data in the internet of things era, and 3D memory architecture is required. 3D flash memory encompasses numerous pillars that punch through control gate plates, and cells are arranged along the pillars [1]. We refer to each pillar as a memory hole. Memory holes are fabricated by dry etching of stacked films, which are generally constructed of dozens to several hundred pairs of SiO2/Si or SiO2/Si3N4 films. Therefore, the aspect ratio of a memory hole must be strictly controlled because these features at each control gate plate directly affect the characteristics of memory cell. Therefore, the key technology of 3D flash memory is a high aspect ratio (HAR) hole etching process. However, the dry etching process of HAR holes has a variety of profile issues, including bowing, shape distortion, twisting of the hole profile, and striation.

In this study, sidewall striation formation in a HAR hole was investigated. In spite of the smooth morphology of the mask, sidewall striation was observed on dielectric films. Results from the carbon mask sample treated with several gas plasmas implies that ion irradiation can increase the degree of striation on the carbon mask, and striation tends to be suppressed by deposition of a fluorocarbon film from fluorocarbon radicals. An ion beam experiment with a simulated hole sidewall using blanket films shows that striation tends to form on the fluorocarbon film rather than on SiO2 and Si3N4 films. In connection with this result, the shallower region with striation had thicker fluorocarbon film than the deeper region with smooth sidewall. Therefore, the possible of sidewall striation formation mechanism is as follows. When the etching depth of the HAR holes reaches a certain depth, striation forms on the deposited fluorocarbon film and is transferred to the dielectric films laterally as the hole diameter increases. The region with striation depends on the aspect ratio, defined as the depth divided by the neck width of the carbon mask. Consequently, as etching progresses, the mask thickness decreases and striation forms in a deeper region, depending on the aspect ratio.

References

[1] H. Tanaka et al., Symposium on VLSI Technical Digest, 14 (2007).

5:00pm **PS+EM-TuA-9 Plasma Processing of Phase Change Materials**, *Ernest Chen*, *N Altieri*, University of California, Los Angeles; *C Neumann*, *S Fong*, *H Wong*, Stanford University; *M Shen*, *T Lill*, Lam Research Corporation; *J Chang*, University of California, Los Angeles

The manipulation of the amorphous to crystalline phase transition observed in chalcogenide glasses for non-volatile memory applications has been studied for many years since its initial conception. However, only recently has innovation in both materials development and memory device architecture enabled phase change random access memory (PCRAM) to become a promising candidate for applications such as neuromorphic computing. Ternary chalcogenide glasses consisting of germanium, antimony, and tellurium are widely used in PCRAM applications, and Ge₂Sb-₂Te₅ (GST-225) will be the focus of this study.

Understanding the effects of plasma processing on the phase change material (PCM) utilized in PCRAM is crucial to ensuring proper device performance. The studies presented in this talk utilize a custom-built integrated system equipped with ion beam processing, downstream plasma processing, quadrupole mass spectrometry, optical emission

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spectroscopy, and x-ray photoelectron spectroscopy capabilities. The samples are prepared by sputtering from a stoichiometric GST-225 target. Prior studies have examined the behavior of GST-225 when exposed to different components of ambient exposure (N₂, O₂, and H₂O) as well as H₂ and CH₄ discharges and identified H₂ and CH₄ as capable GST etchants.

It is known that ambient exposure will cause a GST-225 layer to be oxidized in the first several nanometers, and this oxidized layer has different properties from the bulk of the GST-225 film and may also behave differently from the bulk material when exposed to plasma processing. Initial studies with *ex-situ-* XPS analysis indicate that H₂ can etch GST-225 with approximately 5% change in composition (5% increase in Ge, 5% decrease in Sb, approximately 0% change in Te) and a significant change in the ratio of 0+ to X+ (non-oxidized to oxidized) bonding states between the oxidized surface and the etched surface. In order to distinguish the effects of plasma processing on the oxidized layer and the bulk material, a custombuilt downstream plasma processing chamber integrated with an XPS chamber is used. This system allows for the study of the surface states of GST-225 post-processing without any inadvertent effects from ambient conditions that may complicate *ex-situ* XPS analysis.

5:20pm PS+EM-TuA-10 Meeting the Challenges in Patterning Phase Change Material for Next Generation Memory Devices, Meihua Shen, L Thorsten, J Hoang, S Chiou, D Qian, A Routzahn, J Chen, A Dulkin, J Sims, A McKerrow, R Dylewicz, Lam Research Corporation INVITED Phase change materials (PCM) have emerged as the leading candidate for next generation non-volatile memory device with unique characteristics that significant differ from conventional DRAM and NAND flash memory. Recently, 3-D Cross point PCRAM, for example, has transitioned into high volume production, demonstrating a non-volatile memory product exhibiting faster speed, low voltage operation and high density.

Phase change materials are typically chalcogenide alloys containing elements such as Ge, Sb, Se, Te with various dopants. The materials exhibited phase change between amorphous insulating state and the crystalline conductive state under thermal/electric heating. To ensure electric device performance, it is critically important to maintaining the PCM elemental composition and structure integrity during patterning. The challenges of patterning PCM come from the soft nature of the material and the damages that can easily occur during plasma dry etch, ambient air exposure, wet clean and encapsulation process. To meet the challenges, we developed an integrated system combining dry etch, wet clean and ALD encapsulation modules together. In this paper, we will present the comprehensive studies on each module as well as the interactions of the modules in successful patterning of the phase change materials. The discussions will be focused key learnings on how to maintain the feature fidelity and the integrity of the materials during etch and encapsulation.

6:00pm **PS+EM-TuA-12 Utilizing Photosensitive Polymers to Estimate UV Radiation Exposures in Different Plasma Chamber Configurations,** *Luxherta Buzi, M Sagianis, S Engelmann,* IBM T.J. Watson Research Center Monitoring vacuum ultraviolet (UV/VUV) emission in plasma systems is challenging as it requires specialized diagnostic systems or sensors to be compatible with reactive ion etch (RIE) tooling. This study is mapping different reactor configurations with various levels of UV emission and its effect on a known set of polymers.

Photon-induced modifications on polymers can help decouple ion and photon effects on materials therefore, the impact of inductively coupled and microwave plasma configurations on etch rates and chemical properties of photoresists were investigated. Poly(methyl methacrylate) and Poly(4-hydroxystyrene)-based photoresists were deposited on Si wafers and exposed to argon (Ar) and nitrogen (N₂) plasmas which generate different levels of UV irradiation. X-ray Photoelectron Spectroscopy (XPS) and Fourier Transform Infrared (FTIR) were used to analyze the polymer composition and molecular structure and the surface roughness was analyzed with an atomic force microscope (AFM).

FTIR and XPS confirmed that N₂ plasma effects on chemical modifications were more pronounced on the Poly(methyl methacrylate). Roughness and etch rate was significantly higher for Poly(methyl methacrylate) compared to Poly(4-hydroxystyrene)-based photoresists. Detailed elemental and molecular structure analysis of polymers showed relatively higher damage caused from the inductively coupled plasma, which is ultimately correlated to a higher UV emission.

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