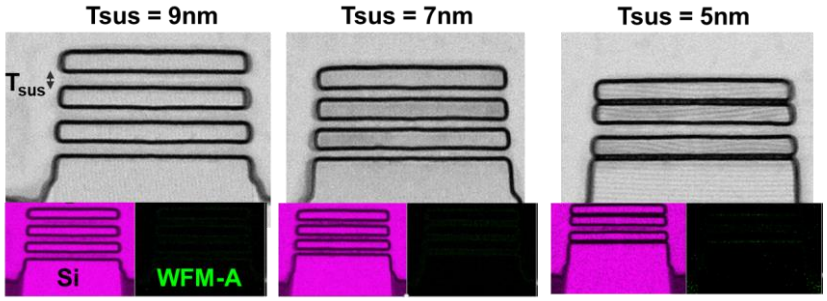

Fig. 1: TEM micrographs (*inset:* EDS map of Si, WFM-A) post gas phase dry etch of WFM-A. TEMs show structural feasibility post etch and EDS confirming complete etch of WFM-A. Si channel collapse at T_{sus} = 5nm can be explained from TEM sample preparation.

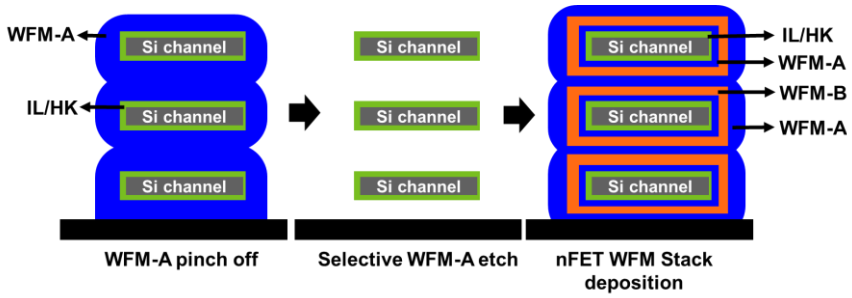

Fig. 2: Schematics and process sequence for nFET WFM patterning with selective WFM-A etch followed by re-deposition of the nFET WFM stack

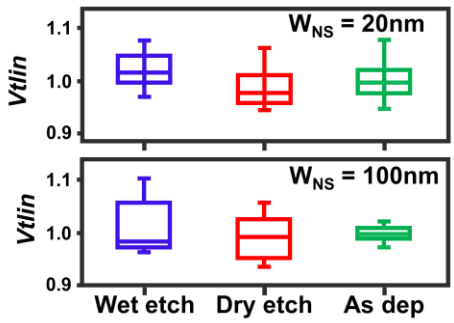

Fig. 3: Comparing V_{tlin} from W_{NS} 20 and 100 nm from WFM-A etch using wet etch, our dry etch and no etch "as-deposited" by ALD. L_g = 100nm for all.

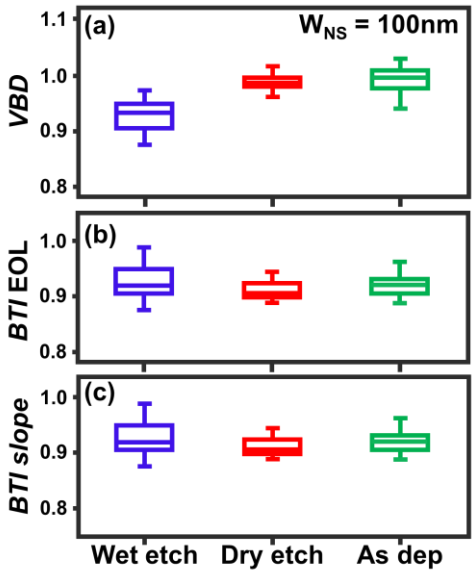

Fig. 4: Comparing device performance impact (a) VBD, (b) BTI, (c) BTI slope, from WFM-A using wet etch, our dry etch and no etch "as-deposited" by ALD. W_{NS} = 100nm, CPP 100nm and L_g = 100nm.

[1] K. J. Kuhn, *Trans. Electron Devices*, 2012, 59, 7, pp.1813. **[2]** D. Nagy et al, *IEEE J. Electron Devices Soc*, 2018, 6, pp.332. **[3]** H. Mertens et al, *IEDM*, 2016, pp. 524. **[4]** N. Loubet et al, *VLSI*, 2017, pp.T230. **[5]** N. Loubet et al, *ECS Meeting Abstracts*, 2018, 31, pp. 1075. **[6]** N. Loubet et al, *IEDM*, 2019, pp. 242. **[7]** J. Zhang et al, *IEDM*, 2017, pp. 537. **[8]** R. Bao et al, *IEDM*, 2019, pp. 234.