Manufacturing Science and Technology Group
Room 305 - Session MS+HI-MoM

Machine Learning for Microelectronics Manufacturing Process Control and Materials Discovery R&D

Moderators: Tina Kaarsberg, U.S. Department of Energy, Advanced Manufacturing Office, **Gary Rubloff**, University of Maryland, College Park

8:20am **MS+HI-MoM-1 Advancing Semiconductor Industry Process Control via Data-Centric AI*, Jeff David,*** PDF Solutions **INVITED**

Data-Centric AI.Over the last several decades, much of the research and work in machine learning has been based on a model-centric approach or software centric approach.[1] In recent years, some of the codebase for core algorithms such as neural networks have reached a level of maturity where those base algorithms now essentially represent a solved problem for a lot of applications.This has created the opportunity to focus more on the data to improve results, where there is still a significant amount of room to improve the approaches to boost overall outcomes.Areas of Data-Centric AI that have received a growing amount of attention recently include[1]: Measuring data quality, Data iteration, Data management tools, and Data augmentation and data synthesis.

While there has been increasing application of Data-Centric AI in other industries, there are also opportunities for the application of Data-Centric AI in the semiconductor industry as well.Below are a two examples of approaches that have been explored and implemented:

Metabinning and generalized model across chip products

It is difficult to train a model using available data that can be applied to other chip products, due to the unique bin assignment across potentially many thousands of products, even though the underlying failure mechanisms at the device level may be similar.A solution to this challenge is to create metabins that group together bin ID's that are the same or very similar, across chip products.By generating metabins as new labels and overriding the original hardbin/softbin ID's (which again may be disparate), a generalized model can be trained with more previously available data and quickly applied to new chip products for failure prediction.

Classification of wafer failure patterns

Key difficulties in applying machine learning to the classification of spatial failure patterns on wafers are the limited number of wafer classifications (labels) and wafer data available to train the model for a new chip product.To address these issues, a Data-Centric AI approach can be applied.The first step is to generate Augmented Data: Wafers with known patterns are generated randomly.Then the new patterns can be quickly added to the model, by expanding the pattern definition library and retraining.Unlike actual data, new patterns from one product type might be considered general learning and useable to upgrade models.

References:

(1)Andrew Ng, NeurIPS Workshop, Data Centric AI, December 2021

9:00am **MS+HI-MoM-3 Paths Toward Autonomous Plasma Process Tool Operation by Pairing of Plasma and Machine Learning Technologies*, Jun Shinagawa,*** *P. Ventzek,* Tokyo Electron America Inc., **INVITED**

"Smart manufacturing" initiative is a means to meet automation and process control requirements set by semiconductor device technology that is now far below the 10 nm critical dimension in manufacturing[1]. We present our holistic approach on pairing first principle in-situ plasma diagnostics with machine learning techniques to build key components of autonomous plasma process tool operation system or advanced equipment control (AEC) system. AEC is a multi-module system consisting of plasma monitor and control and fault detection and classification(FDC) modules. Machine learning techniques are used to enhance accuracy and reliability of embedded models in the aforementioned modules.

REFERENCE

[1] SEMI, "What is smart manufacturing?" [Online], Available: https://www.semi.org/en/industry-groups/smart-manufacturing/what-is-smart-manufacturing [Accessed Nov. 30, 2021]

9:40am **MS+HI-MoM-5 Compliant Hybrid Bonding for Large CTE Mismatched Electronic Materials*, Mieko Hirabayashi Hirabayashi,*** *M. Wiwi, S. Herrera, E. Madison, M. Jordan,* Sandia National Laboratories

We will discuss methods for hybrid bonding utilizing low modulus materials to enable heterogeneous integration with high density (< 20 µm pitch) interconnections of CTE (coefficient of thermal expansion) mismatched materials. Hybrid bonding techniques, where mechanical stability is provided from a direct bond and electrical connection through a metal-to-metal bond are used to make high-density electrical connections for materials like hybridized CMOS imagers. The temperature of formation of the direct bond and the stiffness of the bonding material result in highly stressed interfaced, limiting the materials that can be used for a hybrid bond.

We demonstrate the joining dissimilar materials utilizing a compliant bonding layer. By changing materials, we allow stress moderation in the bonding layer which reduces the stress on the top and bottom chips. Reliability decreases significantly when the differences in coefficients of thermal expansion (CTE) are large. With large CTE mismatch between a top chip and a bottom chip, one chip expands more than the bottom chip during thermal cycling. If the interface is brittle, the stress due to the difference in CTE induces cracking at the interface. The current method for addressing this issue is to limit the total area bonded –but this limits the advancement of the technology.

This has ramifications for infrared imagers and other applications that combine compound semiconductors with silicon microchips. The size of hybridized infrared imagers, for example, is limited by the mismatch between the different materials that go into them. This presentation will include the methods we have developed to integrate polymers between dissimilar materials to reduce stress due to CTE mismatch and thus increase reliability.

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10:40am **MS+HI-MoM-8 Machine Learning Accelerated Scale-up for Microporous Materials - An Industrial Perspective*, Di Du,*** *P. Kamakoti,* ExxonMobil Technology and Engineering Company **INVITED**

Microporous materials such as zeolites and MOFs play a crucial role in producing energy and energy products at scale. Traditional approaches for materials development and scale-up are time consuming and involve experience-based trial and error. Two key areas for materials understanding are the critical variables that impact the synthesis and optimization of material properties which are usually described by quantitative synthesis-property relationships (QSPR). This presentation provides an overview of statistical and machine learning approaches to build QSPR. These methods provide a highly efficient path to optimize synthesis parameters towards targets such as purity, crystal size and surface area, and enable us to significantly speed up our materials workflow.

Our workflow combines design of experiments, machine learning, and high-throughput experimentation (HTE). In order to build QSPR, we featurized the characterization data using machine learning and deep learning approaches. For example, we quantified crystal purity using peak deconvolution of powder XRD pattern. We used a deep learning model to calculate crystal size and aspect ratio from scanning electron microscopy (SEM). We performed functional principal component analysis to select the linear region of Brunauer-Emmett-Teller (BET) adsorption curve which is found to be more accurate than Rouquerol's rules. Since the synthesis space for microporous materials is large and complex, we combined Bayesian Optimization and HTE to further accelerate the workflow. The prior knowledge for Bayesian optimization often comes from a sparse matrix. We used an iterative machine learning model to predict and fill the missing values with uncertainty quantification. After optimization, we used feed-forward neural networks to summarize QSPR for extended investigation at different scales.

We validated the accelerated workflow with a known zeolite. Without referring to historical data, we used the workflow to systematically probe a large and complex synthesis parameter space and obtain small pure crystals of the material. The new workflow demonstrated a significant reduction in the number of experiments needed to meet the same goals as past experiments.

11:20am **MS+HI-MoM-10 Optimizing Copper Deposition in High Aspect Ratio Through Silicon Vias***, **Jessica N. McDow**, R. Schmitt, M. Hirabayashi, J. McClain, M. Jordan,* Sandia National Laboratories

We show an optimization method for filling high aspect ratio through silicon vias (TSVs) that provides insights into the diffusion and suppression kinetics of a superfilling electroplating chemistry. In general, TSV copper filling processes are designed to be used with thinned wafers (<200 µm), but some TSV last and microelectromechanical systems (MEMS) require full wafer thicknesses. To electroplate full-wafer thickness TSVs, a suppressor only solution utilizes an s-shaped negative differential resistance (S-NDR) mechanism.[1,2]

This suppression/fill mechanism is sensitive to the via geometry as well as the overpotential during the electroplating. Using a suppressor only chemistry consisting of copper sulfate, sulfuric acid, potassium chloride, and Tetronic 701, we demonstrate a time-dependent process window where early on too high of an overpotential results in suppressor breakdown and too low of an overpotential results in complete suppression of the deposition process. By controlling the voltage between -520 mV (MSE) and -560 mV (MSE), we were able to demonstrate complete fill of the TSVs in 30% of the time previously required for filling. We also hypothesize that there is a maximum void-free fill rate for suppressor only chemistries.

Understanding the filling kinetics provides a throughput target for microelectronic devices. Copper filled TSVs are a key technology for 3D heterogeneous integration. TSV designs improve device functionality, increase bandwidth per volume, simplify assembly, and enable system miniaturization. In this work, understanding of copper deposition kinetics in a suppressor only electrolyte and the development of optimized plating parameters utilizing the S-NDR mechanism is outlined.

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[1]Rebecca P. Schmitt et al 2020 J. Electrochem. Soc. 167 162517.

[2]D. Josell and T. P. Moffat 2018 J. Electrochem. Soc. 165 D23.

11:40am **MS+HI-MoM-11 Advanced Manufacturing using Virtual Metrology and Equipment Intelligence®** *, **David Fried**,* Lam Research Corporation **INVITED**

The semiconductor industry is now confronting a number of metrology and manufacturing challenges due to critical technology requirements at next-node architectures.Advanced patterning techniques, such as EUV, frequency multiplication and selective deposition, are needed to meet cost and variability challenges at smaller line dimensions.Memory technologies, such as NAND, DRAM, and others, are requiring new materials and the transition to 3D topologies that are more challenging to manufacture.Advanced logic (such as GAA architectures) and heterogenous integration are being pursued in order to reduce power, footprint, and speed in next generation devices, but also require new, higher density and more complex manufacturing techniques.These technology requirements are creating additional metrology challenges, such as a need to measure smaller dimensions in complex 3D structures, increased measurement frequencies and additional demands for metrology data integration and analysis.

In this talk, we will discuss innovative concepts to address some of these next node metrology challenges.We will review the concepts of virtual fabrication and virtual metrology, and how they can be used in conjunction with conventional metrology to better support defect analysis and yield optimization at the latest technology nodes.We will also discuss how physical metrology can be used to calibrate a virtual process model, along with how a virtual process model can be used to validate physical metrology measurements made on a 3D NAND device.

In addition, our presentation will review the concept of Equipment Intelligence®, and how sensor-based metrology is being used to improve chamber and fleet variability.We will discuss how data from in-situ and standalone metrology, using machine learning/artificial intelligence, calibrated models, and advanced analytics, can drive real-time feed-forward and feedback optimization. We will show a specific example of next-generation metrology-based optimization, by presenting an advanced, in-situ etch-depth metrology system that uses spectral analysis and machine learning to deliver significant improvements in wafer-to-wafer etch depth control.

In our conclusion, we will summarize the challenges of next node architectures, and discuss how the concepts discussed in this presentation can be used by all participants in the semiconductor technology space to measure, characterize and address these upcoming challenges.

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