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Low Energy Ion Beam Backside Circuit Edit Applications in FinFET Devices

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Circuit Edit (CE) using Focused Ion Beams (FIB) has been widely adopted in the industry to validate known circuit and design marginality issues, test circuit design changes, and generate engineering samples [1]. An approach, commonly known as backside CE, is to access the transistor cell and lower level interconnects of interest through the bulk silicon. The highly localized FIB milling continues until Shallow Trench Isolation (STI) region or the transistor fins are exposed. This FIB exposed trench is commonly referred to as a Node Access Hole (NAH) and it is within this area that subsequent CE tasks such as, accessing, cutting, or rerouting of lower level signals take place [2]. At the most commonly used ion beam energy of 30 KeV, Ga^+ Ion beam penetration depth, can negatively affect circuit performance by altering the intrinsic device parameters. In order to preserve the functionality of the neighboring active devices, machining geometries need to be limited by the transistor cell size and ion beam material interaction volume

An obvious approach in reducing ion material interaction volume is to operate at lower ion beam energy [3]. At reduced beam energy, the lateral machining geometry can increase in size due to reduction in the ion material interaction range. In a FinFET device, the transistor channel is located at the tip of the fin, 50 to 70 nm from the bulk substrate –STI interface. Sufficient reduction in the ion beam material interaction volume also allows non-invasive machining directly over-active transistors.

In this work, we present a new approach in using low energy Ga^+ Ion beams at 5 KeV energy for NAH preparation. At low ion beam energy, we demonstrated that the NAH dimension is no longer limited by the cell size. We will present simulation data on interaction volume of the ion beams relative to the depth of the channel in FinFET, showcasing the effectiveness of low energy Ga^+ beams. Finally, we will present empirical results measuring timing impact of ion beam machining on free running ring oscillator test structures and will show example edit results on latest generation process node devices.

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