The energy efficiency of microsystems improved by more than 1000x every 20 years under Dennard scaling, where shrinking the linear dimension of a transistor while maintaining a constant electric field scaled the frequency and the voltage of operation. Satisfying the continued demand for computing, when scaling is projecting a single doubling of energy efficiency over the next 15 years, will require innovation across algorithms, architectures, and devices. Sandia has established programs pursuing the basic research underlying probabilistic neuromorphic computing, reconfigurable architectures, energy-efficient AI at the edge, and material manipulation for fine-grained integration of sensing and computation. In this talk, I will focus on a specific transistor that circumvents the physical limitation that ended Dennard scaling, and lowers the operating voltage of a circuit.

Tunnel field effect transistors (TFETs) rely on band-to-band tunneling, and promise a 10x improvement in energy efficiency compared to metal oxide semiconductor transistors (MOSFETs), all while maintaining the same materials. They have not achieved this promise due to poor on:off current ratios, and smeared dopant profiles producing gradual turn-on currents. We have designed a TFET in a vertical geometry which uses atomic precision advanced manufacturing (APAM) to form the buried electrode and the intrinsic tunnel barrier. This design boosts current by scaling with the area of the device instead of a 1D edge and obviates limitations from the abruptness of the doping profile. However, APAM has traditionally only been used to fabricate qubits, and has little to do with microelectronics.

Here, we integrate APAM with conventional fabrication, providing a straightforward path both to advanced transistor devices that work in practical conditions, and to scaled manufacturing. We first demonstrate both the two halves of the vertical TFET device operating at room temperature. We show an APAM nanowire integrated with common back end of line processing, which reveals the APAM nanowire strongly confines carriers, leading to current densities that exceed that of copper. Next, we demonstrate the gated top half the TFET device, limiting processing to thermal budgets tolerated by APAM. The low-thermal budget MOS transistor is used to evaluate the quality of APAM material. Next, we demonstrate integration into a CMOS fabrication flow, complete with working hybrid APAM-CMOS circuits. Finally, we explore operational robustness by showing that CMOS features fail before APAM features in accelerated lifetime testing.

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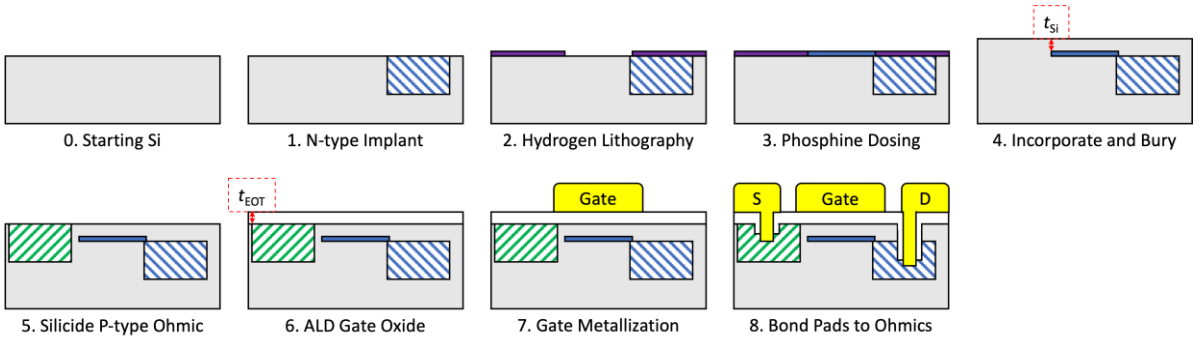

Figure 1. Process flow for fabricating APAM-based TFET, including callouts of the important silicon thickness and oxide thickness variables. Top row defines the bottom layer of the TFET, while the bottom row defines the top layer of the TFET. We show transport data from both halves of the device in Figure 3.

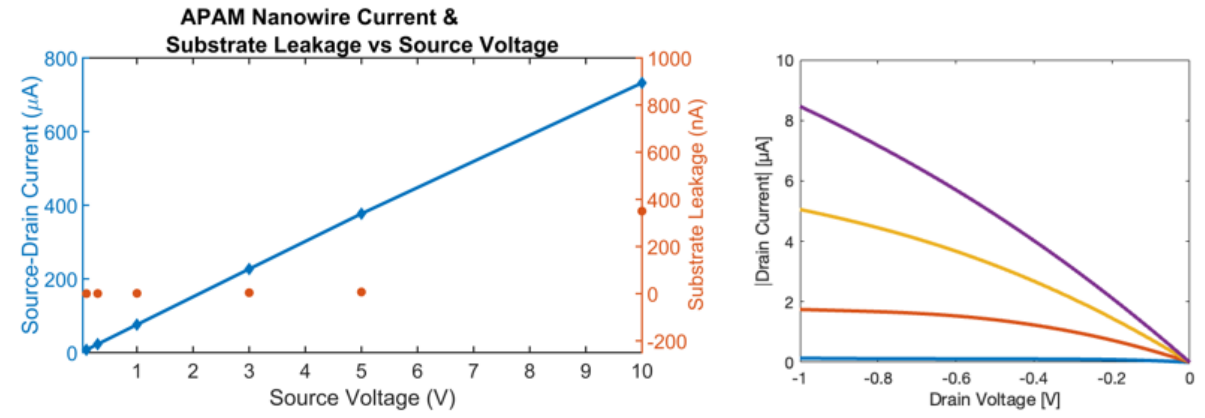

Figure 2. Room temperature electrical transport through both the bottom half (left) and top half (right) of the TFET shown in Figure 1, demonstrating the viability of the device concept.

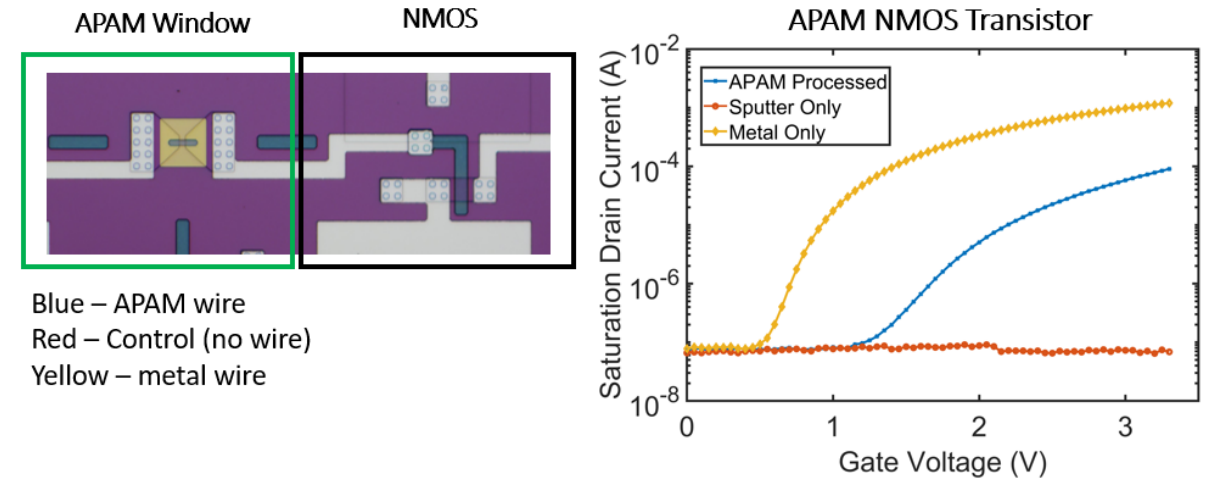

Figure 3. Demonstration of a manufacturable APAM process integrated in the middle-of-line with CMOS.