Manufacturing Science and Technology
Room Central Hall - Session MS-ThP

Manufacturing Science and Technology Poster Session

MS-ThP-1 Novel Inspection Technology for Detecting Via Open Using Parallel E-beam Scanning and Graphic Design System, ***Chihoon Lee***, SSIT (Samsung Institute of Technology), Republic of Korea

As dual-damascene Cu interconnect technique is currently being employed for on-chip interconnect fabrication, and will continue to be used for next technology generations due to significant cost advantage [1]. In this process, however, it has been challenging to detect via open defects occurring in the underlying layer after the completion of the Cu metal line. A viable in-line monitoring to detect via open defects in the back-end of line (BEOL) has been challenging due to the complex multiple via structures connected to the metal line. Today's conventional inspection method do not meet the requirements of a true in-line monitoring strategy [2]. Despite detecting the dark voltage contrast (DVC) signal as a via open defect in the conventional electron beam (E-beam) inspection system, it was not genuine defects in most cases by the transmission electron microscopy (TEM) analysis for detected via open defects. We guess that it is attributed to the complexity of the vertically designed BEOL metal/via structures, which makes it difficult to separate exact via open location in the upper and lower layers. Figure 1 shows exactly detected via open defect image and related metal/via layout with E-beam inspection system.Early in-line detection of these via open defects prior to the electrical die test is crucial for yield improvement. In this talk we demonstrate a novel inspection technology to detect the critical BEOL via open defects using parallel E-beam scanning and graphic design system (GDS). Parallel E-beam scanning is an inspection technique that can detect more electrons by adjusting the stay time of electrons according to the shape of the metal line pattern. It was controlled by the landing energy (LE), scan direction in the E-beam inspection system. In addition, the detecting locations of via open were restricted near single via layout using die to database (D2DB) inspection system to improve the detectability. It can effectively capture the signals of via open defects compared to the conventional E-beam inspection in the complex high dense metal/via structures.

[1] A. V. Vairagar et al., Appl. Phys. Lett. 87, 2005

[2] M. Daino et al., *28th Annual SEMI Advan. Semiconductor Manuf. Conference (ASMC)*, 2017

MS-ThP-2 EES2: Advancing Microelectronics and Computing Energy Efficiency Through a Co-Design Approach, ***I-Hsi Daniel Lu***, Energetics

The U.S. Department of Energy's (DOE) Energy Efficiency Scaling for Two Decades (EES2) initiative is a pioneering effort aimed at achieving a 1000x improvement in energy efficiency in all aspects of computing over the next two decades. This ambitious goal is based on the concept of doubling energy efficiency every two years—a new type of scaling—leading to a 1000x over two decades. EES2 focuses on operational efficiency in computing, —from hardware components to software elements.The roadmap leverages an integrated, interdisciplinary co-design approach to optimize energy use across the entire compute stack. Recognizing that the natural slowing of efficiency gains due to factors like the end of Dennard scaling challenge the industry, EES2 emphasizes the importance of co-design, where adjacent layers of hardware and software are developed in tandem to achieve energy efficiency by orders of magnitude without trading off performance.

The roadmap challenges the industry to achieve these ambitious efficiency goals, stimulating innovation and discussion by identifying key technologies that can serve as benchmarks. Through a series of near-, mid-, and long-term strategies, EES2 prioritizes energy efficiency in every aspect of design and development in Microelectronics. Central to this version 1.0 of the EES2 effort are eight working groups: Materials and Devices, Circuits and Architectures, Advanced Packaging and Heterogeneous Integration, Algorithms and Software, Power and Control Electronics, Metrology and Benchmarking, and Education and Workforce Development. These groups work collaboratively to ensure that the layers of the compute stack enhance energy efficiency, by using co-design as one of the approaches.

As EES2 expands its focus to include emerging technologies such as quantum computing and photonics, the initiative aims to return to or exceed the historical pace of energy efficiency enabled by Dennard scaling by innovations and set new benchmarks for the industry. This poster will explore the collaborative efforts among industry, academia, and national laboratories that underpin this initiative, emphasizing the transformative potential of the co-design approach in driving energy efficiency advancements in microelectronics.

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