Plasma Science and Technology
Room 124 - Session PS1-TuM

Plasma Processes for Advanced Memory

Moderators: John Arnold, IBM Research Division, Albany, NY, **Jeffrey Shearer**, TEL

8:00am **PS1-TuM-1 Control of High Aspect Ratio Dielectric Etch Profile using Additive Etching Gases***, **Hyun Woo Tak**, C. Choi, M. Park, J. Lee, B. Kim, J. Jang, E. Kim, D. Kim, G. Yeom,* Sungkyunkwan University (SKKU), Republic of Korea

To form high-density memory devices, high aspect ratio contact (HARC) etching is critical as it determines the integration density of memory devices. Given that there is no standardized definition of "high" in high aspect ratio, it is crucial to continuously improve the HARC etching capability to meet the requirements of next generation memory devices. In this study, the effects of various additive etching gases added with only a few standard cubic centimeters per minute (sccm) flow rates on etch characteristics of HARC structures were investigated. It is found that, by using a few sccm of various fluorine, sulfur and metal containing gases added to the process gases, etch characteristics such as etch selectivity, etch profile, and pattern charging can be controlled during the HARC etching. Detailed results on the effects of these gases such as etch rates, selectivity, and profiles, assessed through scanning electron microscopy (SEM) analyses will be provided in the presentation. Moreover, to understand the etch mechanism, the plasma and surface characteristics after addition of the additive gases were investigated by optical emission spectroscopy (OES), quadrupole mass spectrometry (QMS), and X-ray photoelectron spectroscopy (XPS). This research demonstrates that small additive gases in addition to main etch gases can significantly affect next-generation HARC etching processes, paving the way for advanced memory device fabrication.

8:15am **PS1-TuM-2 Experimental and Molecular Dynamics Simulation Study of W and WSi Hard-Mask Etching by Fluorocarbon Plasmas***, **Hojun Kang**,* Osaka University, Japan, Republic of Korea*; S. Kawabata,* Osaka University, Japan*; N. Mauchamp,* Osaka University, Japan, France*; E. Tinacba,* Osaka University, Japan, Philippines*; T. Ito,* Osaka University, Japan*; S. Kang, D. Lee, J. Son,* Samsung Electronics, Republic of Korea*; K. Karahashi, S. Hamaguchi,* Osaka University, Japan

In response to the growing demand for high-density memory devices, driven by the advancement of smartphones, data centers, and AI technologies, the development of efficient fabrication techniques for complex structures of DRAM and 3D NAND devices has become increasingly critical. This necessitates the enhancement of plasma etching capabilities with high-energy ions, especially the development of mask materials with little erosion under high-energy ion irradiation. This study aims to clarify the etching characteristics of W-based hard masks under SiO_2 etching conditions with fluorocarbon plasmas. W-based hard masks are among the candidate materials to replace conventional Si or C-based hard masks. With a mass-selected ion beam system[1], W and WSi sample surfaces were irradiated with high-energy Ar^+ and CF_3^+ ions ranging from 500 to 4000 eV, with an ion dose of $1\sim2\times10^{17}$ ions/cm^2. After ion irradiation, etched depths were measured with a surface profiler, and the etching yields were evaluated. Changes in the surface atomic compositions and chemical bonding were assessed through ex situ X-ray photoelectron spectroscopy (XPS). The depth profiles of the atomic composition below the etched surfaces were also measured with XPS employing 1,000 eV Ar^+ ion etching. Our findings indicate that, below 1,000 eV, CF_3^+ ions exhibit lower etching yields on W-Si masks compared to Ar^+ ions; however, this trend reverses at energies exceeding 2000 eV. At lower energies, the formation of a W-C mixed layer inhibits the etching yield. Molecular dynamics (MD) simulations were also performed to evaluate the beam-surface interactions. The simulations used an embedded atom method (EAM) interatomic potential functions for W-W interactions [2], and Stillinger-Weber (SW)-type interatomic potential functions for W-C and W-Si interactions developed in this study. The study found good agreements between the experimental findings and simulated data. The force fields developed in this study allow further MD simulation of challenging etching scenarios that are hard to investigate by experiments only, such as etching with high incident angles, various ion energies, and high-aspect-ratio (HAR) etching with sidewall effects. This study underscores the potential of W-based hard masks in next-generation memory fabrication, offering critical insights into the surface reactions essential for optimizing the etching processes, supported by both experimental and simulation data.

References

[1] K. Karahashi, et al., J. Phys. D: Appl. Phys. **47**, 224008 (2014)

[2] D. R. Mason,et al., J. Phys.: Condens. Matter **29** 505501 (2017)

8:30am **PS1-TuM-3 3D NAND Dielectric Etch Technology Challenges and Breakthrough***, **Youn-Jin Oh**, T. Lill, M. Wilcoxson, T. Kim, H. Singh,* Lam Research Corporation **INVITED**

Three-dimensional NAND technology has revolutionized the landscape of memory storage, enabled higher capacities and improved performance in semiconductor devices. However, the fabrication of 3D NAND structures presents unique challenges, particularly in the plasma etching. This presentation explores the challenges of plasma etching encountered and the indispensable role of new chemistries in cryogenic etch processes.

In 3D NAND device manufacturing, the vertical stacking of memory cells increases continuously, and lateral scaling has been tightened simultaneously, which brings more challenges to plasma etch process.The introduction of cryogenic etch has been able to breakthrough the critical challenges of vertical etch rate, mask selectivity, and critical dimension (CD) control, which enable us to scale up continuously.

In the cryogenic etch process, the role of chemical interactions on surfaces emerges as pivotal.In this presentation, the process breakthrough with various new chemistries will be discussed on the high aspect ratio SiO_2/Si_3N_4 (O/N) stacks in a capacitively coupled plasma (CCP) etcher which has high power, dual frequency, and high conductance capabilities.How cryogenic process performance is optimized with the synergy between new chemistries and advanced plasma modulation techniques will also be presented.

9:00am **PS1-TuM-5 Patterning Challenges of Thick Tungsten Carbide Hard Mask Layers***, **Daniel Montero**, K. Katcko, F. Lazzarino,* IMEC, Belgium

Newer technology nodes are increasingly demanding the patterning and integration of High aspect ratio vias (HAR) with increasing aspect ratios (AR) to meet stricter chip design requirements. For some fields, as in memory applications, it comes at the cost of increasing the stack height to accommodate more memory layers, while in logic patterning, a reduction in the via critical dimension (CD) may also be necessary. High AR vias are challenging structures to pattern from the plasma etch point of view, as it requires a precise control of the plasma parameters to pattern straight HAR vias, while reducing the bowing, undercut and hard mask consumption. For most applications using HAR vias, the target layers to pattern are dielectrics, which require the use of a long plasma etch process, and hence a highly selective hard mask (HM) layer able to resist this process. Most hard mask layers may lack enough selectivity to achieve the desired dielectric HAR via patterning quality in terms of selectivity, bowing and uniformity.

Our previous work [1] demonstrated that Tungsten Carbide (WCx) HM layer may exhibit higher selectivity than other HM in Back End of Line applications. However, the results derived in [1] cover the development of thin WCx layers (up to 15 nm thick) for line-space patterns. In this work, we extend and detail the etch development of thick WCx layers, up to 350 nm thick, in the context of HAR via 3DNAND memhole patterning applications. Our test vehicle uses immersion lithography at 193 nm to pattern staggered vias at 480 nm pitch into a 1 µm thick silicon oxide layer, with expected AR of 8.0 and 5.3 for 60 and 90 nm CD vias respectively.

In a first approach, we used Continuous Wave (CW) plasma, derived from [1], with an adapted etch time to pattern the 350 nm thick WCx layer, but it showed limited performance. Hence, a redevelopment of the plasma etch process was needed to guarantee uniform, straight, and complete opening of the thick WCx HM layer. Different passivation and etching methods, as well as the use of Synchronized Pulsed Plasma, are proposed to improve the patterning performance of WCx layers. Then, the 300 mm wafers continue processing towards the oxide etch, and selectivity to WCx HM is evaluated. The results are then compared to the reference HM of the test vehicle, Amorphous Carbon Layer (ACL). WCx HM showed better selectivity and lower corner erosion than the ACL reference layer, proving that WCx layers may be a valuable candidate for HAR via patterning in 3DNAND memhole applications.

Refences: [1] D. Montero et al, *Exploring the use of Tungsten-based Hard Masks in BEOL interconnects for 3nm node and beyond.* AVS68 2022.

9:15am **PS1-TuM-6 Sheath Uniformity with Pulsed Low Frequency Biases for High Aspect Ratio Plasma Etching***, **Evan Litch**, M. Kushner,* University of Michigan

Current roadmaps for microelectronics fabrication place focus on fabrication of 3-dimensional devices for higher functionality requiring increasing high aspect ratio (HAR) features. 3D-NAND memory structures containing hundreds of alternating layers of SiO_2 and Si_3N_4 require etching of vias having aspect ratios (ARs) exceeding 100. Deep trench isolation (DTI) for electrical isolation have similar HAR challenges. DTI etching of conductive substrates using halogen gas mixtures (e.g. HBr/Cl_2) is typically performed in inductively coupled plasmas (ICPs) with a substrate bias to facilitate highly anisotropic etching.

Plasma etching of HAR features requires ion energy and angular distributions (IEADs) that are high in energy, more than several keV, and narrow angular distribution. These requirements motivate the use of very low frequency biases (VLF) – 100s kHz. Concurrently, there is a transition to using pulsed biases to optimize the ratio of radical to ion fluxes. One of the motivations for pulsing is to gain the advantages of high peak power that produces higher energy ions with narrow angle distribution while lowering the average power deposition. However, pulsing at higher voltages thicken the sheath while low frequencies charge focus rings (FR), that can lead to significant sheath curvature at substrate boundary thereby modifying IEADs away from desired characteristics.

In this presentation, results will be discussed from a computational investigation of IEADs incident onto wafers and remediation of edge exclusion when using pulsed VLF biases in ICPs for etching of trenches for DTI and TSVs (through silicon vias).Simulations were conducted using the Hybrid Plasma Equipment Model (HPEM). Operating conditions are tens of mTorr mixtures of $Ar/Cl_2/O_2$ with bias frequencies from 250 kHz to 5 MHz. Bias voltages are up to a few kV with pulse repetition frequencies of up to 10s kHz. The consequences of these operating conditions on etching DTI and TSV features were evaluated using the Monte Carlo Feature Profile Model (MCFPM). When using continuous wave biases, the charging of the FR is sensitive to frequency, and this charging produces sheath curvature at the edge of the wafer, which perturbs IEADs. With pulsed biasing, the FR is transiently charged both during the VLF cycle and during the pulsed cycle, adding additional challenges to minimizing edge exclusion. Comparisons for different reactor/FR properties will be discussed.

This work was supported by Samsung Electronics Co. and the US National Science Foundation (2009219).

9:30am **PS1-TuM-7 Study of Electrode Material Effects on High Aspect Ratio SiO_2 Etching in CCP Etch Systems***, **Chanhyuk Choi**, H. Tak, S. Kim, M. Park, J. Lee, B. Kim, J. Jang, E. Kim, D. Kim, G. Yeom,* Sungkyunkwan University (SKKU), Republic of Korea

In semiconductor memory device manufacturing, plasma etching, particularly for high aspect ratio contact (HARC), has become increasingly crucial. A significant challenge is the uneven polymer deposition on the sidewalls of structures, leading to ion tilting, charging effects, and pattern distortion. Recent advancements have focused on integrating conductive materials, especially tungsten (W) by using WF_6 as an additive gas. WF_6 gas addition to the process gases has been effective in forming conductive polymers that resist etching, improving etch profiles, thus enhancing precision in etching. This study examines the use of a different showerhead material in addition to Si showerhead as an upper electrode with DC voltage for etching, comparing it to the traditional showerhead made of Si to assess their impacts on etching properties.

The SiO_2 etch rate was increased for all showerheads used in the experiment with increasing DC voltage, while the amorphous carbon layer (ACL) etch rate was remaining constant, indicating enhanced selectivity. The Si showerhead showed minimal improvement in removing charging with increased voltage, whereas the other showerhead significantly enhanced the bottom etch profile due to improved charge related issues. That is, Si showerhead showed bottom hole distortion, and which was not improved with increasing DC voltage to the showerhead while the other showerhead showed improved bottom hole shapes and profiles at higher DC voltages indicating improved charging related issues. XPS also showed a higher showerhead material atomic percent (at%) on the substrate for the -600V process compared to the 0V process when using the other showerhead, indicating more conductive polymer formation during the etching.

The etching with the other showerhead showed more anisotropic and undistorted etch profiles of ACL masked SiO_2 holes compared to the etching with Si showerhead due to lower charging related issues during the SiO_2 etching with polymer forming fluorocarbon gases due to the formation of more conductive polymer on the substrate during the etching. This research provides new insights into the role of electrode material reactivity in advanced etching processes of high aspect ratios in CCP systems.

9:45am **PS1-TuM-8 Low GWP and Low Emission Gases for High Aspect Ratio Etching Application***, **Scott Biltek**, N. Stafford, P. Nguyen, F. Qin,* Air Liquide*; P. Forest,* Air Liquide, France

Over the past few years, numerous countries and semiconductor manufacturing entities have unveiled their commitments to achieving net-zero carbon emissions by 2050 or even sooner. When it comes to manufacturing chips, plasma etch processes contribute significantly to emissions, especially in dielectric etching. High aspect ratio structures are commonly used in both memory (3D NAND and DRAM) as well as logic chip manufacturing processes. These structures are traditionally etched using fluorocarbon and hydrofluorocarbon gases to etch very challenging dielectric structures. Unfortunately these gases, such as C4F8, CH2F2, CHF3, CF4, etc have very high Global warming potentials (GWP) along with other gases like C4F6 and CH3F which have low input GWP but potentially high GHG emissions.

However, while there has been a significant amount of work over the years to develop alternative low GWP etching gases, it is not only difficult to incorporate these chemistries in such very challenging etch processes but also understanding the emitted species from the plasma into the exhaust is rather limited. As the plasma dry etching is an extremely complex process involving chemical bond dissociation, recombination, side reactions, etc it is difficult to predict with any accuracy the post plasma exhaust stream and thus the CO2 equivalence of the plasma byproducts.

In this work we will present novel low GWP etching gases to replace traditional high GWP gases such as C4F8 and CHF3/CH2F2 that not only give improved etching performance but reduce the CO2 equivalent (CO2 eq) emissions from the etch chamber exhaust. This work utilizes Fourier Transform Infrared Spectroscopy (FTIR) to measure the exhaust stream of a 300mm CCP plasma etch chamber. Finally, we will present an etching recipe exclusively composed of low GWP etching gases.

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