MEMS and NEMS
Room 125 - Session MN2-TuM
Heterogeneous Integration and Packaging

Moderators: Robert Davis, Brigham Young University, **Vikrant Gokhale**, Naval Research Laboratory

11:00am **MN2-TuM-13 Advanced Packaging Driven Heterogeneous Integration***, **Robert Patti**,* NHanced Semiconductors Inc **INVITED**

Introduction

Semiconductors are an amazing success story. Since their introduction in 1959 they have found their way into every segment of our lives – transportation, entertainment, medicine, communication, weaponry, etc.At each step the chips became smaller, faster, cheaper, and more powerful, in a progression known as Moore's Law.

Today, Moore's Law is slowing and the industry's path forward is less well defined.This paper introduces a new concept, Foundry 2.0™, that offers fresh solutions for the future.

Current Challenges

Scaling

Shrinking the transistors no longer produces inevitable gains. Each new node is more difficult and expensive to achieve and some elements, notably capacitors, actually perform more poorly at smaller sizes. Meanwhile, wiring is approaching its physical limits, consuming a larger share of the power and signal time and generating problematic capacitance.

Size and Yield

One solution to the scaling problem is to cram more functionality onto each chip. The resulting system-on-chip (SoC) dies are powerful but physically larger, which translates directly to poorer yield. In addition, all functionality is necessarily built in the same processes, which imposes compromises.

Cost vs. Innovation

The cost and complexity of today's leading-edge chips dictates that they be manufactured in vast quantities to achieve economies of scale. Customization is out of the question and innovation is greatly constrained.

Foundry 2.0™ Solutions

Foundry 2.0™ is a manufacturing model that takes dies and chiplets from high-volume foundries and applies advanced packaging (AP) and other back-end-of-line (BEoL) processes to create specialized devices at lower volumes. Foundry 2.0 does not attempt to replace the existing industry, but to transform it. It does not compete with the high-volume leading-edge foundries; it works with them to penetrate the smaller markets where customization is prized.

As a neutral party, the Foundry 2.0 manufacturer can source its dies from any major foundry. Best-of-class components can be selected regardless of node, substrate, manufacturing process, or source, and then combined in 3D stacks or 2.5D assemblies that precisely fill the needs of specific markets.

By avoiding the high cost of building transistors Foundry 2.0 can economically produce smaller lots. Its high-mix low-volume model addresses markets that high-volume fabs simply cannot afford to accommodate. Foundry 2.0 makes innovation profitable again.

11:30am **MN2-TuM-15 Advances in Reliability Monitoring and Failure Analysis in Three-Dimensional Microsystems***, **Matthew B. Jordan**, M. Bahr, L. Basso, A. Mounce, A. Ferris, J. McDow, J. Christiansen, J. Walraven, W. Mook,* Sandia National Laboratories*; J. Lee,* University of Central Florida*; A. Jarzembski, W. Hodges, J. Carroll, B. Young, G. Pickrell, L. Yates, J. Neely,* Sandia National Laboratories

Three-dimensional, heterogeneous integration of microsystems has introduced new failure mechanisms while making it more difficult to screen and diagnose those failures. High-consequence applications require accurate reliability estimates; thus, we have developed *in-situ* reliability monitors for continuous surveillance. Furthermore, when components fail, we need to locate and characterize the failure mechanisms. To that end, we have adapted and developed novel failure analysis techniques for use in 3D microsystems.

In this manuscript we present two reliability monitors designed to provide granular detail on the state of health of a 3D microsystem. The first generalizes daisy-chain analysis methods based on network flow. The individual 3D interconnects are treated as vertices in a network where when they are cut it alters the maximum flow through the network. In this way, data on the failure rate of individual interconnects can be accurately determined with a smaller set of tests than a standard daisy chain where the network is severed after a single failure. The second reliability monitor is an *in-situ* strain gauge based on the Si piezoresistive effect allowing for localized measurement of the fatigue of 3D microsystems.

Secondly, we will discuss some methods used to localize and characterize failures in 3D microsystems. As we cannot access the surface of the components as we would in a planar system, we must rely on subsurface probing methods. The first of these methods is frequency domain thermoreflectance (FDTR), which utilizes a pump/probe laser system to characterize the thermal interfaces of a 3D microsystem. We find with FDTR that after sufficient sample preparation, small changes in microbumps can be resolved based on their thermal transport properties. Secondly, EM field analysis as nitrogen-vacancy in diamond based magnetic field measurements and scanning electric field measurements have been utilized to determine short-circuit and open circuit defects. Lastly, electrical frequency has been used to characterize components as they age (power spectrum analysis).

Guaranteeing the reliability of 3D microsystems is crucial for high-consequence systems. Monitoring system reliability and effectively localizing and analyzing failures are essential for providing this guarantee.

This work was supported by the Laboratory Directed Research and Development program at Sandia National Laboratories. SNL is managed and operated by NTESS under DOE NNSA contract DE-NA0003525.

Author Index

Bold page numbers indicate presenter