Thin Films
Room 206 B W - Session TF+CPS+MS+EM-ThM
Thin Films for Microelectronics I

Moderators: Elton Graugnard, Boise State University, **Robert Grubbs**, IMEC Belgium

8:00am **TF+CPS+MS+EM-ThM-1 Pushing the Limits of Vertical NAND Storage Technology with ALD-based Ferroelectrics***, Prasanna Venkatesan,* Georgia Institute of Technology*; **Asif Khan**,* Georgia Institute of Technology, USA **INVITED**

Solid-state drives (SSDs) continue to serve as the foundation of long-term active data storage in modern data centers. Over the past decade, conventional vertical NAND (vNAND) technology has achieved a remarkable 50× increase in storage density, enabled by advances in physical scaling (x–y and z dimensions) and logic scaling (from multi-level cell, MLC, to quad-level cell, QLC). The explosive growth of artificial intelligence (AI)—with models like GPT-4 surpassing a trillion parameters—has further accelerated the demand for high-capacity, high-performance storage systems to support petabyte-scale datasets.

Today's state-of-the-art vertical NAND devices offer densities nearing 30 Gb/mm^2 with over 300 stacked layers. However, extending this scaling trajectory to 1000 layers and beyond—targeting storage densities exceeding 100 Gb/mm^2—poses significant challenges. Chief among these are reliability concerns intrinsic to charge-trap flash technologies, such as lateral charge migration and the poor endurance of higher logic level operations.

To overcome these limitations, ferroelectric field-effect transistors (FeFETs) have emerged as a promising alternative, enabling further z-direction scaling with improved reliability. This presentation will highlight recent advances in atomic layer deposition (ALD)-based ferroelectric gate stack engineering, and how these innovations can support the development of next-generation NAND architectures capable of 1000-layer integration and ultra-high-density storage.

8:30am **TF+CPS+MS+EM-ThM-3 Electrical Properties of BaTiO3 Thin Films Prepared by Atomic Layer Deposition***, **Jiayi Chen**, Asif Khan, Mark Losego,* Georgia Institute of Technology

This talk will discuss our efforts to develop a robust atomic layer deposition process (ALD) to create ferroelectric $BaTiO_3$ thin films. Ferroelectric materials are potential candidates for future low voltage RAM and NAND memory because of their reversible two polarization states under low external electric field. While the CMOS compatible gate dielectric materials HfO_2 and $Hf_{0.5}Zr_{0.5}O_2$ are ferroelectric, they have high coercive fields that make it difficult to lower switching voltages below 1 V. Therefore, perovskite ferroelectric materials, like $BaTiO_3$ are desirable to use for these applications because their coercive voltages can be an order of magnitude lower, approaching 0.1 V. However, these ferroelectric films must be deposited by ALD to match the conformality and small thickness requirements desired for RAM and NAND memory. This talk will present the electrical properties of $BaTiO_3$ thin films deposited by an ALD process using Bis-(1,2,4 triisopropylcyclopentadienyl)-Barium and Titanium Isopropoxide precursors. We are able to achieve dielectric constants as high as 15 in as-grown (non-crystalline) thin films, and 140 in annealed (crystalline) thin films, with low leakage current (10^{-4} A / cm^2 at 3 V). Specifically, we will focus on the variations of dielectric constant and leakage current as we optimize deposition recipe, $BaTiO_3$ thin films' stoichiometry, scale down the thickness from 50 nm to 10 nm, and measure at cryogenic and elevated temperatures. We will also discuss the implications of these measurements, and the possible route to achieve ferroelectric $BaTiO_3$ thin films by ALD.

8:45am **TF+CPS+MS+EM-ThM-4 Interlayer-Modulated Coercive Field in $HfZrO_2$ Ferroelectric Devices***, **Marshall Frye**, John Wellington-Johnson, Lance Fernandes, Prasanna Ravindran, Asif Khan, Lauren Garten,* Georgia Institute of Technology

Ferroelectric NAND (FeNAND) using $Hf_{0.5}Zr_{0.5}O_2$ (HZO) offers increased memory density, speed, and decreased operation voltage of NAND compared to charge trap flash technology.[1] However, to compete with charge trap flash, the memory window of FeNAND must be increased above 6 V for 3 bit/cell operation or above 8 V to enable 4 bit/cell operation.[1] Since the memory window is directly related the ferroelectric coercive field (E_c), finding pathways to increase the coercive field of HZO is critical to enable FeNAND. Prior studies show that inserting a dielectric interlayer can increase the coercive field, but the mechanism driving the increase in E_c beyond just adding a capacitor in series is still unclear.[2]

The goal of this work is to test the hypothesis that the increased defect states in the dielectric-HZO interface cause in-built fields that then increase the coercive field.[3] First, we fabricate 19 nm HZO both with and without Al_2O_3interlayers or adjacent layers. Varying the layer thicknesses and positions via atomic layer deposition allows for the determination of how the device structure impacts the ferroelectric switching. Polarization-electric field hysteresis loops and positive-up-negative-down (PUND) show ferroelectric switching for each of the films, with a remnant polarization ($2P_r$) up to 27.4 μC/cm^2. The coercive field increases from 1.01 MV/cm in devices without an additional dielectric layer (19 nm HZO) to 3.11 MV/cm in a 3 nm Al_2O_3 interlayer inserted between two 8 nm layers of HZO (8 nm HZO-3 nm Al_2O_3-8 nm HZO). First-order reversal curve (FORC) analysis reveals an increase in internal bias field in devices with dielectric layers, potentially due to defects at the Al_2O_3 - HZO interface. X-ray photoelectron spectroscopy valence band measurements confirm an increase in mid-gap defect states at this interface compared to bulk of the film. Additionally, temperature-dependent modulus spectroscopy is used to evaluate the activation energy and defect concentration in samples with and without a dielectric layer. These findings provide key insights into mechanisms to modulate coercive field in HZO, enabling the design of FeNAND devices with larger memory windows.

References

[1] G. Kim et al., *J. Mater. Chem. C* **2022**

[2] L. Fernandes et al., *IEEE Trans. Electron Devices* **2025**

[3] D. Das et al., *Int. Electron Devices Meet. IEDM*, **2023**

9:00am **TF+CPS+MS+EM-ThM-5 Towards Low-Resistance p-Type Contacts to 2D Transition Metal Dichalcogenides Using Plasma-Enhanced Atomic Layer Deposition***, **Ageeth Bol**,* University of Michigan, Ann Arbor **INVITED**

One major limitation of 2D transition metal dichalcogenide (TMD) based FETs is the high contact resistance between metallic electrodes and semiconducting channels, particularly for p-type contacts. In this presentation I will address how PEALD of p-type TMDs can be used to improve this contact resistance. First, I will go over controlled doping strategies to form p-type 2D TMD contact materials using PEALD, with an emphasis on Nb Doped WS_2. Our recent results show contact resistancevalues as low as 0.30 ± 0.26 kΩ·μm between Pd and PEALD NbxW1-xS2, demonstrating that low resistance contacts between metal and p-type TMDs are possible. Then, I will discuss reducing unintentional p-doping introduced during PEALD of TMDs. PEALD TMDs typically contain some level of hydrogen impurities that leads to unintentional p-doping. We have shown that these impurities can be reduced by introducing an Ar plasma C step in the standard PEALD TMD process. Finally, the use of remote plasmas in PEALD for contact deposition can lead to the creation of undesired impurities and defects in the 2D TMD channel, possibly impacting electronic behavior. I will present some first insights into the defects that are created during PEALD on 2DTMDs and how we can reduce the number of plasma-induced impurities and defects.

9:30am **TF+CPS+MS+EM-ThM-7 Self-Limiting Atomic Layer Deposition of Few-Layer MoS_2***, **Sungjoon Kim**, Jeffrey Elam,* Argonne National Laboratory

Computational energy consumption has been increasing exponentially, making energy-efficient microelectronics and computing an urgent need. Three-dimensional integrated circuits (3D ICs) and neuromorphic computing promise to revolutionize information technology by drastically reducing the energy consumption of computers, and two-dimensional (2D) semiconductors like molybdenum disulfide (MoS_2) can enable such technologies. However, scalable and controllable manufacturing processes are still needed to realize the technology's full potential. Here, we demonstrate the uniform and controlled deposition of few-layered MoS_2 using atomic layer deposition (ALD) for the purposes of memtransistor fabrication. By leveraging the equilibrium shift from material deposition to material etching, a self-limiting deposition of MoS_2 is achieved where material growth is stopped after the initial few layers. The resulting few layer MoS_2 was characterized using Raman spectroscopy and X-ray photoelectron spectroscopy, and was used to fabricate and test memtransistors. This deposition strategy is straightforward, robust and more scalable compared to other methods such as powder CVD and exfoliation.

9:45am **TF+CPS+MS+EM-ThM-8 DOE's Energy Efficiency Scaling for Two Decades (EES2): Featuring ALD-Fabricated Microelectronics Devices for Ultra-Energy-Efficient Computation at Argonne National Laboratory**, ***Emilie Lozier,*** U.S. Department of Energy, Advanced Manufacturing Office; *Jeffrey Elam,* Argonne National Laboratory; *Desiree Salazar,* Energetics; *Tina Kaarsberg,* U.S. Department of Energy, Advanced Manufacturing Office

Electricity demand in the U.S. is projected to grow ~2% annually, potentially reaching a 50% increase compared to today by 2050 (International Energy Agency 2025). A major driver of this growth is the rise of energy-intensive AI computation, according to a bottom-up analysis of data center energy use published by Lawrence Berkeley National Laboratory (LBNL) in December 2024. Including cryptocurrency mining, LBNL's report projects that data-center-based computation could account for roughly a quarter of total U.S. electricity consumption by 2028. While efforts are underway to increase generation to the grid, any solution must simultaneously address the energy efficiency of compute if it is to be successful. Kicking off three years ago, the U.S. Department of Energy (DOE) Advanced Materials and Manufacturing Technologies Office (AMMTO) has already been leading a multi-organization effort united around the shared aim of advancing ultra-energy-efficient compute technologies. This collaborative effort, known as the Energy Efficiency Scaling for Two Decades (EES2) initiative, is uniquely situated to take on this energy challenge. Through EES2, DOE/AMMTO has convened eight working groups representing more than 70 voluntarily pledging organizations across industry, academia, nonprofits and the National Labs to draft an R&D Roadmap describing technologies-to-beat to achieve biennial energy efficiency doubling for the compute stack compounding to a 1,000X efficiency increase by 2040. Moreover, Version 1.0 of the R&D Roadmap (available here: https://eere-exchange.energy.gov/FileContent.aspx?FileID=f4234e29-cc0c-4a56-a510-86b616ab5535) has spurred a suite of EES2-identified and DOE-funded research projects to pursue some of the most promising technologies for enabling ultra-energy-efficient computation. This presentation will highlight one such project at Argonne National Laboratory – with collaborators at Stanford University, Northwestern University, and Boise State University – that has been advancing two-dimensional semiconductor field-effect transistors (2D-FETs) and memtransistors, both fabricated with atomic layer deposited (ALD) molybdenum sulfide (MoS_2) with potential to achieve 50X and 10,000X energy efficiency improvements, respectively. Along with timely project updates, this presentation will also discuss how the Argonne project will integrate with the finalized Version 1.0 of the EES2 R&D Roadmap, that is due to be published in the second half of 2025.

11:00am **TF+CPS+MS+EM-ThM-13 Integrated Magnetoacoustic Isolator with Giant Non-Reciprocity**, *Bin Luo, Benyamin Davaji,* ***Nian-Xiang Sun,*** Department of Electrical and Computer Engineering, Northeastern University **INVITED**

Recent advances in integrated nonreciprocal components—such as isolators and circulators—have enabled transformative wireless communication and sensing technologies, including full-duplex radio, in-band self-interference cancellation, and protected high-power transmission systems. While commercial ferrite-based isolators offer low insertion loss and high power handling, their reliance on kOe-level bias fields, high-temperature ferrite growth, and bulky permanent magnets severely limits their compatibility with CMOS processes and low-power applications.

To address these limitations, magnetoacoustic isolators have emerged as a promising class of passive, CMOS-compatible, and power-efficient nonreciprocal devices. These isolators consist of magnetic heterostructures integrated within the propagation path of surface acoustic waves (SAWs) on piezoelectric substrates. Magnetoelastic and magnetorotational coupling mechanisms enable strong spin wave–acoustic wave interactions, generating hybrid magnetoacoustic waves with dramatically asymmetric damping rates in opposite directions. This asymmetry yields unidirectional transmission, fundamental to nonreciprocal operation.

Despite progress, early devices suffered from weak non-reciprocity, primarily due to a mere helicity mismatch effect and an inherent symmetric spin wave dispersive relation in single-layer magnetic films. Recent efforts have focused on engineering magnetic stacks with nonreciprocal spin wave dispersion. Key examples include: (i) **interfacial Dzyaloshinskii–Moriya interaction (iDMI) stacks** like CoFeB/Pt, (ii) **interlayer dipolar-coupled (IDC) stacks** such as FeGaB/SiO_2/FeGaB, and (iii) **RKKY synthetic antiferromagnets** like CoFeB/Ru/CoFeB. These architectures achieve nonreciprocity strengths up to 250 dB/mm. Recent demonstrations using shear-horizontal waves in $LiTaO_3$ substrates coupled to ferromagnetic and anti-magnetostrictive bilayers have yielded nonreciprocity levels of 60–82 dB/mm with simpler fabrication.

Nevertheless, a persistent challenge remains in reducing insertion loss while maintaining wide bandwidth and high isolation. We will introduce our recent efforts in a **fundamental mode SAW-driven** magnetoacoustic isolator with **giant non-reciprocity** and a **wideband nonreciprocal** magnetoacoustic isolator based on **non-collinear dipolar-coupled ferromagnetic stacks**. The talk will provide a comprehensive overview of the mechanisms, material platforms, and experimental breakthroughs driving the field of magnetoacoustic isolators. We will highlight the path toward integrated, low-loss, and high-performance nonreciprocal components for future quantum, RF, and IoT systems.

11:30am **TF+CPS+MS+EM-ThM-15 Stress Control and Thermal Stability of a FeCo-Ag Multilayer Thin Films for Use in Magnetoelectric Heterostructures**, ***Thomas Mion,*** *Konrad Bussmann,* US Naval Research Laboratory

This investigation studies the stress control and thermal properties of FeCo/Ag multilayer thin films prepared by sputter deposition for their potential applications in magnetoelectric heterostructure devices. While development of magnetoelectric devices has increased, the practical implementation of magnetic thin films is often confounded by additional processing and packaging steps which can be detrimental to the quality of the magnetic film and subsequently the performance of the device. We show the annealing of the FeCo/Ag multilayers is robust until annealing temperatures reach 300 – 400 C where a breakdown of the Ag leads to an increased coercive field, and annealing >400 C is severely detrimental to the soft magnetism of the system as the Ag layers deteriorate. Additionally, as-deposited stress can play a dominant role in micromechanical devices when released. We will show the stress control of this ferromagnetic thin film through in-situ substrate bias allows the films to be tailored from a broad range of +320 MPa tensile to -300 MPa compressive with application of up to a -120 VDC bias during deposition.

11:45am **TF+CPS+MS+EM-ThM-16 Extraordinary Magnetoresistance in High-Mobility $SrTiO_3$ Thin Films**, ***Zhifei Yang,*** *Shivasheesh Varshney,* University of Minnesota; *Sreejith Sasi Kumar, Tristan Steegemans, Rasmus Bjørk, Dennis Valbjørn Christensen,* Technical University of Denmark; *Bharat Jalan,* University of Minnesota

Magnetoresistive sensors are widely used to detect magnetic fields by measuring changes in electrical resistance. One such effect, extraordinary magnetoresistance (EMR), arises from the geometry of semiconductor-metal hybrid structures that combine high-mobility semiconductors with highly conductive metals. EMR strongly depends on both the semiconductor's mobility and the quality of the metal-semiconductor contact (ohmic contact with low contact resistance). The device geometry further influences boundary conditions and current paths under magnetic fields, enabling flexible design and performance tuning. While most previous EMR studies have focused on III-V semiconductors and 2D materials, there has been limited exploration of oxide-based systems.

Here, we demonstrate EMR in high-quality La-doped $SrTiO_3$ thin films grown on $SrTiO_3$ (001) substrates using hybrid molecular beam epitaxy (MBE). We grow films with carrier concentrations ranging from ~2×10^{17} cm^{-3} to ~1×10^{20} cm^{-3}, achieving Hall mobilities from ~300 $cm^2/(V\cdot s)$ up to over 50,000 $cm^2/(V\cdot s)$ at 1.8 K. Using an asymmetric device geometry that breaks mirror symmetry between voltage probes, we observe corresponding asymmetry in magnetoresistance (MR) measurements. With embedded metals that are ohmic contacts to $SrTiO_3$, we achieve an MR ((R(B) – R(0))/R(0), where R(B) is the measured resistance at magnetic field B) approaching 9000% at 9 T and 1.8 K, which is over 3900% higher than the intrinsic MR of $SrTiO_3$ – a *world record* for an oxide-based EMR device! Finite element simulations of current flow and MR in these $SrTiO_3$-based hybrid structures align well with experimental data, validating the design principles. These results establish the potential of complex oxide systems for low-temperature EMR sensors and open opportunities for integrating oxide heterostructures in future magnetoelectronic devices. In this presentation, we will discuss the hybrid MBE growth and microfabrication of high-mobility $SrTiO_3$ thin films, along with device optimization strategies and detailed magnetotransport measurements across various temperature and magnetic field ranges.

12:00pm **TF+CPS+MS+EM-ThM-17 Examining the Spin Structure of Altermagnet MnTe Epilayers Grown by Molecular Beam Epitaxy**, ***Qihua Zhang***[1], The Pennsylvania State University; *Mingyu Yu,* University of Delaware; *Alexander Grutter, Christopher Jenson, William Ratcliff, Julie Brochers,* National Institute for Science and Technology (NIST); *Narendirakumar Narayanan, Thomas Heitmann,* University of Missouri; *Nitin Samarth, Stephanie Law,* The Pennsylvania State University

As a new class of magnetic materials, altermagnets feature alternating arrangement of magnetic moments with zero net magnetization, a typical characteristic of an antiferromagnet; yet they also feature large spin splitting in its electronic band structure. NiAs-phase (α-) MnTe has gained significant attention as a candidate of altermagnet family owing to its large spin-splitting energy and high transition temperature. In this study, we investigate the altermagnet properties of MBE-grown α-MnTe layers using neutron diffraction experiments. We first study and optimize the growth conditions of MnTe layers grown directly on InP (111)A substrates. It is seen that using a lower growth temperature result in a narrower full-width-at-half-maximum (FWHM) in the x-ray diffraction (XRD) rocking curves, but will introduce whiskers on the surface, while increasing the Te/Mn flux ratio improves both the crystalline quality and the surface morphology. With a temperature window of 250-400 °C and a Te/Mn flux ratio of 3, we further obtain high quality α-MnTe films with a 0.8 nm surface roughness and a corresponding threading dislocation density of ~7.5×10^{8} cm^{-2}. Temperature-dependent neutron diffraction measurements were performed on the MnTe films grown with optimized conditions. A fitted Néel temperature of 304 K was obtained based on the half-order antiferromagnetic peak along the (0001) direction, which confirmed the bulk-like antiferromagnetic behavior in the α-MnTe. Using polarized neutron reflectometry, substantial spin asymmetry is captured while very small net magnetization (up to 4 emu/cm^3) across the MnTe layer is obtained, highlighting a near-to-ideal stoichiometric α-MnTe. Angle-resolved photoemission spectroscopy is further used to confirm the spin splitting in the eletronic band structure. This study carefully clarifies the magnetic band structure in a promising altermagnet candidate and introduces potential methods of controlling the ferromagnetism in the materials.

[1] **TFD Distinguished Technologist Award**

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