Atomic Scale Processing Mini-Symposium
Room 316 - Session AP+EL+PS+TF-WeM

Thermal and Plasma Enhanced Atomic Layer Etching

Moderators: Eric A. Joseph, IBM Research Division, T.J. Watson Research Center, **Erwin Kessels**, Eindhoven University of Technology, the Netherlands

8:00am **AP+EL+PS+TF-WeM-1 Cyclic dielectric etching challenges for next-generation FDSOI logic and quantum devices**, ***François Boulard***, CEA-LETI, France; *Ramy Ayoub,* CEA-LETI, France, Lebanon; *Emmanuel Petitprez, Stéphane Pocas, Nicolas Gauthier, Benoit Martin, Pierre Brianceau, Antoine Ronco,* CEA-LETI, France; *Bernard Pelissier,* LTM-CNRS, France; *Nicolas Posseme,* CEA-LETI, France **INVITED**

As logic devices dimensions scale down(1) and quantum gates advance in scalability and environment resilience(2), the demand for gentle, selective, and highly controlled fabrication processes has become critical. Atomic-scale processing—particularly cyclic approaches like Atomic Layer Etching (ALE) and quasi-ALE—has emerged as a potential solution. By leveraging fluorocarbon-based chemistries in sequential deposition/removal cycles, these methods have already demonstrated superior performances in terms of SiO_2 to Si_3N_4 selectivity, such as in Self-Aligned Contact (SAC) etching(3). While the fundamental mechanisms of these cyclic processes are increasingly well understood(4), their industrial applicability—especially for advanced integration schemes—still faces challenges in versatility, robustness, and throughput. In this presentation, we will highlight recent advances in adapting cyclic etching strategies to selectively etch dielectric materials (SiO_2, SiON, Si_3N_4) for two cutting-edge applications: Contact multipatterning in next-generation FDSOI CMOS logic devices and intertwined gate patterning for cryogenic FDSOI quantum chips. This study explore the critical role of process parameters, including fluorocarbon precursor selection, multi-step cyclic strategies, substrate temperature and plasma power modulation, and their collective influence on etch per cycle stability, selectivity, uniformity, throughput, and pattern transfer fidelity.

By bridging fundamental insights with integration-driven optimization, this work clears the path to highly scalable, atomic-precision etching—a key enabler for both classical and quantum semiconductor technologies.

The research work presented in this paper was carried out in the framework of the FAMES Pilot Line of the Chips JU, funded by Horizon Europe grant 101182279 and the ANR NextGen project ANR-22-NEXTG001 of the France 2030 initiative. Part of this work, carried out on the Platform for Nanocharacterisation (PFNC), was supported by the “Recherche Technologique de Base” and "France 2030 - ANR-22-PEEL-0014" programs of the French National Research Agency (ANR).

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(2)B. Bertrand, et.al., International Electron Devices Meeting, IEDM 2023, DOI: 10.1109/IEDM45741.2023.10413763

(3)M. Honda, et.al, 2017, J. Phys. D: Appl. Phys. 50 234002 [tel:50 234002], https://doi.org/10.1088/1361-6463/aa6f27

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8:30am **AP+EL+PS+TF-WeM-3 Atomic Layer Etching of TiN using O_2/Ar Plasma and SF_6/H_2/Ar Plasma Half-Cycles**, ***Kazuya Tajima,*** Hitachi High-Tech Corporation, Japan; *Andrew P. Kaye,* Colorado School of Mines; *Kazumasa Okuma, Hiroaki Ishimura,* Hitachi High-Tech Corporation, Japan; *Sumit Agarwal,* Colorado School of Mines

Titanium nitride (TiN) has become a widely adopted material for both logic and memory devices due to its appropriate work function with high-k gate stacks and excellent barrier properties against fluorine and oxygen diffusion. Atomic layer etching (ALE) of TiN was performed by a combination of surface modification by oxidation during the O_2/Ar plasma half-cycle and release of volatile etch products in the SF_6/H_2/Ar plasma half-cycle. [1,2] For the ALE experiments, we used low-resistivity TiN deposited by atomic layer deposition. In the O_2/Ar plasma half-cycle, TiN was oxidized to TiO_x with O radicals. For the SF_6/H_2/Ar plasma cycle, the SF_6-to-H_2 flow ratio was tuned to minimize continuous etching of TiN. Quadrupole mass spectrometry (QMS) was used to identify conditions that maximize the production of HF in the SF_6/H_2/Ar plasma, which acts as the etchant for surface modified TiO_x layer, and does not spontaneously etch TiN. Using QMS, we also identified the primary reaction products produced in each half-cycle. Our data show that NO was the primary nitrogen-containing product in the Ar/O_2 plasma half-cycle. TiF_2^+ and TiF^+ ions were detected by the QMS in the SF_6/H_2/Ar plasma half-cycle, which most likely originate due to cracking of TiF_4 parent molecules in the ionizer. The likely O-containing product during the SF_6/H_2/Ar plasma half-cycle is H_2O, which could not be detected due to the background signal in the QMS. In addition, we also detected SO^+ and SO_2^+ ions during both half-cycles due to the presence of S on the substrate and/or the chamber walls.

The etching process was performed at 200 °C. While the oxidation of TiN was quasi-self-limiting during the O_2/Ar plasma half-cycle, subsequent etching in the SF_6/H_2/Ar plasma half-cycle was not self-limiting. The synergy parameter, *S*, [3] is an indicator of the ideality of the ALE process. We show that the ALE end point could be determined by the time decay of the reaction products measured by the QMS, and the synergy parameter could be optimized by limiting the duration of the SF_6/H_2/Ar plasma half-cycle. We were able to obtain a synergy parameter of ~82% under optimized conditions.

[1]Lee et al., Chem. Mater. 29, 8202 (2017);

[2]Hossain et al., J. Vac. Sci. Technol. A 41, 062601 (2023);

[3] Kanarik et al.,J. Vac. Sci. Technol. A 35, 05C302 (2017);

8:45am **AP+EL+PS+TF-WeM-4 Atomic Layer Etch Process for InGaAs Using (CH4+H2)/Ar+ Plasma**, ***Burak Okur,*** *Ryan Walsh, J. Russell Renzas,* University of Nevada, Reno

Precise, damage-free etching of InGaAs with Angstrom-scale control is a critical requirement for next-generation III-V semiconductor device fabrication, including gate recess etching in InGaAs HEMTs, which require very precise etching of ~20 nm of InGaAs. Conventional plasma etching is insufficiently precise for this application and introduces subsurface damage and surface roughness, motivating the development of atomic layer etching (ALE) processes that achieve controlled material removal through sequential, self-limiting surface reactions.

In this work, we investigate a plasma-based ALE process for InGaAs using $(CH_4+H_2)/Ar^+$ chemistry, consisting of alternating surface modification and removal half-cycles. The expected volatile products are $In(CH_3)_3$, $Ga(CH_3)_3$, and AsH_3. The effects of chamber conditioning, process pressure, and Ar flow rate are systematically investigated to achieve self-limiting ALE behavior. Real-time optical emission spectroscopy (OES) measurements are used to monitor plasma species and investigate the role of residual CH-related species in the transition between self-limiting ALE and RIE-like behavior. For a process at 10 mTorr with 200 W ICP power, 5 sccm Ar, a 1 sec dose of 5 sccm CH_4 and 20 sccm H_2, and 5 sec etch time, an ALE window is present from 10-15 W RF bias, with EPC of 0.25 nm/cycle. The etched surfaces are characterized using scanning electron microscopy (SEM), energy dispersive spectroscopy (EDS), atomic force microscopy (AFM), and profilometry to evaluate etch per cycle (EPC), surface morphology, roughness evolution, and compositional uniformity of the InGaAs surface. Synergy is also measured.

9:00am **AP+EL+PS+TF-WeM-5 O2/CF4/Ar+ 3-Step Plasma Atomic Layer Etch Process for Aluminum**, ***Ryan Walsh,*** *Burak Okur, J. Russell Renzas,* University of Nevada, Reno; *Phuc Pham,* University of Oregon

Aluminum is a light, conductive metal used in an incredible assortment of device fabrication processes, including in superconducting devices, where performance is highly sensitive to material impurities, interface damage, and critical dimensions. Most aluminum reactive ion etch processes use Cl_2 or BCl_3, which have the dual disadvantages of toxicity and post-etch corrosion. Fluorine is not typically used as an etchant for Al films because of the high melting point of AlF_3. It is known, however, that fluorinated AlO_x has a lower sputter threshold than untreated AlOx[1]. We present a novel 3-step plasma Atomic Layer Etch (ALE) process for Al using O_2, CF_4, and Ar^+. This room-temperature cyclical process starts by oxidizing Al in O_2 in Step A. Step B consists of a tetrafluoromethane dose to create an aluminum oxyfluoride modified layer. In Step C, this modified layer is removed via argon ion bombardment, using the oxide as an etch stop for the removal of the more easily sputtered oxyfluoride layer.

EPC of 0.08 nm/cycle and synergy of >99% were achieved with 100 W ICP power and 7 W table bias during step C. Etch control is governed by the thickness of the grown oxide and the depth of fluorine diffusion. We also present AFM, SEM, and XPS to show the effect of this process on the Al surface. This process could provide an avenue toward improved performance in aluminum-based superconducting devices.

[1] Chittock, N. J. (2024). Plasma processes for atomic layer etching. [Phd Thesis 1 (Research TU/e / Graduation TU/e), Applied Physics and Science Education]. Eindhoven University of Technology.

9:15am **AP+EL+PS+TF-WeM-6 Directional Atomic Layer Etching of Lithium Niobate for Nonlinear Integrated Nanophotonics**, ***Ivy Chen***[1], California Institute of Technology; *Frank Greer,* Jet Propulsion Laboratory (NASA/JPL); *Austin Minnich,* California Institute of Technology

Atomic layer etching (ALE) is of intense interest in microelectronics, photonics, and other fields owing to increasing demands for nanofabrication with nanometer-scale precision, aspect-ratio independent etching, and sub-nanometer surface roughness. Nonlinear integrated nanophotonic devices typically employ complex oxides like lithium niobate for which dry etching processes perform poorly. Fundamental improvements in nanofabrication processes are vital to realize the full potential of nonlinear integrated nanophotonics for on-chip quantum information processing and beyond. Here, we report a directional ALE process for LN consisting of sequential exposures of HBr/BCl_3/Ar plasma for surface modification and Ar plasma for removal. We observe an etch rate of 1.04 ± 0.01 nm/cycle with a synergy of 84.6% at a temperature of 0°C. At higher process temperatures, the HBr chemistry is found to decrease redeposition compared to F- and Cl-based plasmas, which we attribute to the higher vapor pressures of Br-based products. A grating pattern etched entirely by the process (total etch depth of 220 nm) exhibits no aspect-ratio dependent etching (ARDE) down to the smallest tested gap of 150 nm, in contrast to ion milling in which ARDE manifests even at 300 nm gaps for the same etch depth. Additionally, we present results on applying our ALE processes to TFLN devices to obtain higher aspect ratios, smoother sidewalls, and precise etch depths, yielding enhanced performance metrics for coupler gratings, ring resonators, and spontaneous parametric downconverters for on-chip quantum information processing.

9:30am **AP+EL+PS+TF-WeM-7 Native Oxide Removal and Passivation of Niobium for Superconducting Devices**, ***Jessica Jones***, Argonne National Laboratory; *Jeffrey Elam,* Argonne National Laboratory, USA

Superconducting materials are foundational to many quantum technologies, yet surface and interfacial disorder remain important barriers to device performance and scalability. In particular, native oxide formation on superconducting metals is believed to contribute to loss and decoherence, creating a need for processing methods that provide precise surface control while maintaining the integrity of the underlying material. Niobium is an attractive superconducting material because of its relatively high critical temperature and broad relevance to quantum circuit platforms. However, complex native oxide formation and near-surface chemical disorder complicate its integration into devices such as Josephson junctions and other superconducting circuit elements. Here, we investigate an atomic-scale surface treatment and passivation approach for niobium thin films aimed at improving control over the metal/oxide interface. Our results show that thermal atomic layer etching can effectively remove native surface oxides from niobium while preserving the underlying metallic surface. Subsequent atomic layer deposition prevents reformation of the native oxide layer on the surface. Together, these findings establish a promising pathway for interface control in superconducting niobium and support the development of improved fabrication strategies for quantum circuit technologies.

9:45am **AP+EL+PS+TF-WeM-8 Thermal Atomic Layer Etching of the Semiconductor Oxide Channel Materials by Sequential Surface Modification and Volatile Release Reactions**, ***Muhammad Hamza Ansar***, *Steven George,* University of Colorado Boulder

Indium gallium oxide (IGO) and Indium gallium zinc oxide (IGZO) can be used as channel materials in metal oxide semiconductor thin-film transistors (TFTs). These TFTs have high carrier mobility, low leakage current and a wider bandgap compared with silicon. Etching the channel material to a precise and controlled thickness is important for device performance. Thermal atomic layer etching (ALE) of these metal oxide semiconductors is possible using surface modification and volatile release reactions.

In this study, the thermal ALE was performed with sequential exposures of boron trichloride (BCl3) and hydrogen fluoride (HF). In situ spectroscopic ellipsometry (SE) measurements on flat films determined etch rates for IGO of 2.1 Å/cycle at 225°C and 3.0 Å/cycle at 255°C. The etch rate for IGZO was 2.5 Å/cycle at 205°C and 5.6 Å/cycle at 255°C. The etch rates were observed to be nearly self-limiting versus the BCl3 and HF exposures.

Quadrupole mass spectrometry (QMS) investigations identified the volatile products during the BCl3 and HF exposures on In2O3, Ga2O3 and ZnO powders. The initial BCl3 exposure reacted with the In2O3, Ga2O3 and ZnO powders and produced InCl3, GaCl3 and ZnCl2, respectively. These products are consistent with conversion to B2O3. The next HF exposure then produced BF3 and H2O from the spontaneous etching of B2O3. The HF then proceeded to yield additional H2O from the fluorination of the metal oxide. The subsequent BCl3 exposure first yielded BF3 from ligand-exchange with the metal fluoride. The BCl3 exposure then proceeded to produce metal chloride by conversion of the underlying metal oxide. The QMS results for Ga2O3 powder are displayed in **Figure 1**.

Additional studies on flat films explored the effect of IGO composition on the etch rate. **Figure 2** shows that the IGO etch rates were 2.8, 3.6, and 4.2 Å/cycle at In:Ga ratios of 1:1, 2:1 and 4:1, respectively at 230 °C. The etch rate then decreased to 0.8 Å/cycle at an In:Ga ratio of 8:1. The thermal ALE was also observed to smooth the initial roughness of the IGZO surface.

11:00am **AP+EL+PS+TF-WeM-13 Isotropic Atomic Layer Etching via Thermal-Cyclic Processing: Broad Material Capabilities with a Focus on Work–Function Metal Films**, ***Kazunori Shinoda***, Hitachi High-Tech Corporation, Japan; *Thi-Thuy-Nga Nguyen, Shunya Hirai,* Nagoya University, Japan; *Nobuya Miyoshi,* Hitachi, Ltd., Japan; *Masaru Izawa,* Hitachi High-Tech Corporation, Japan; *Kenji Ishikawa, Masaru Hori,* Nagoya University, Japan **INVITED**

An isotropic atomic layer etching (ALE) process based on thermal–cyclic processing (thermal-cyclic ALE), consisting of repeated plasma exposure and infrared lamp heating, has been developed for advanced semiconductor manufacturing applications. This approach enables highly controllable and selective isotropic material removal through self–limiting surface reactions driven by cyclic thermal activation. A key advantage of this approach is the independent optimization of the adsorption and desorption temperatures, which enables enhanced material selectivity, improved surface smoothness, and sufficient etch per cycle (EPC). To realize this process at a manufacturing scale, a dedicated 300–mm wafer tool, referred to as a Dry Chemical Removal (DCR), has been developed and commercialized. Using this DCR tool, isotropic ALE processes have been developed for a wide range of materials used in semiconductor device fabrication, including oxides, nitrides, carbides, metals, and compound films. Furthermore, surface reaction mechanisms during the ALE steps have been systematically investigated using in–situ X–ray photoelectron spectroscopy (XPS), providing direct insight into adsorption and desorption steps governing the self–limiting etching behavior. These analyses reveal material–dependent reaction pathways and clarify the roles of plasma–induced surface modification and thermally activated removal of the modified surfaces. This invited presentation provides a comprehensive overview of the thermal–cyclic ALE technology, covering its historical development, process fundamentals, tool design, and mechanistic understanding across multiple material systems.In particular, recent progress in the isotropic ALE of work–function metal films, such as TiC and TiN, will be highlighted, with an emphasis on surface reaction mechanisms investigated by in–situ XPS. These materials are of increasing importance for advanced semiconductor devices, where precise thickness and surface control are critical. Process characteristics and surface chemistry insights obtained by in–situ XPS will be discussed.

11:30am **AP+EL+PS+TF-WeM-15 Selective Thermal Chemical Vapor Etching (CVE) and Atomic Layer Etching (ALE) of Ge Versus Si**, ***Micah Duffield***, *Marcel Junige, Steven George,* University of Colorado at Boulder

The fabrication of gate-all-around nanosheet transistors employs multi-layer stacks of crystalline SiGe and Si. Completely removing sacrificial SiGe and precisely recessing SiGe may be accomplished by chemical vapor etching (CVE) and atomic layer etching (ALE), respectively. Facile Si CVE has been shown previously using anhydrous HF vapor above 150°C. This Si CVE is ceased by co-dosing H_2O+HF. The present work explored selective CVE and ALE pathways for Ge compared with Si using HF only or with oxidants.

Quadrupole mass spectrometry (QMS) measurements identified the volatile etch products during different reactant gas exposures at ramped or isothermal temperatures. Exposing Ge nanopowder to HF during an up-ramp from 25 to 400°C discovered that facile Ge CVE produced volatile GeF_4 at 50-75°C and then turned off due to non-volatile GeF_2 polymer formation. The GeF_2 polymer could then be volatilized at >300°C. Additional experiments at varied ramp rates, a reversed down-ramp, and isothermal HF exposures corroborated this non-volatile GeF_2 polymer formation.

Exposing a mixture of Ge & Si nanopowders to HF during a temperature ramp showed that the GeF_4 etch product in turn etched Si, producing volatile SiF_4 at 75-110°C (**Figure 1a**). Co-dosing H_2O+HF still etched Ge (or GeO_2) and produced volatile GeF_4. However, co-dosing H_2O+HF eliminated the parasitic Si etch pathway via GeF_4 (**Figure 1b**). Introduced H_2O oxidized

[1] **PSTD Coburn & Winters Student Award Finalist**

Si and formed an ultra-thin chemical oxide. This SiO_2 was not etched by GeF_4.

Repeatedly exposing GeO_2 nanopowder to HF at 100°C revealed that GeO_2 etched spontaneously without the self-termination observed for Ge. This finding inspired a unique Ge ALE mechanism: A first oxidant exposure may oxidize Ge to form an ultra-thin GeO_2 surface layer. A subsequent HF exposure may volatilize this GeO_2 surface layer but self-terminate on the underlying Ge due to GeF_2 polymer buildup. The following oxidant exposure may remove the GeF_2 polymer and again oxidize Ge.

Exposing Ge nanopowder to a sequence of oxidant and HF exposures at 100 and 150°C, respectively, revealed that volatile GeF_4 was released after each oxidant exposure in a self-terminating fashion. To refresh the Ge surface after HF exposures, H_2O was ineffective, whereas O_2 was effective, and O_3 was even more effective than O_2 (**Figure 2**). To verify these QMS findings, *in situ* spectroscopic ellipsometry (iSE) studies were employed on Ge thin film samples. Ge ALE using an alternating O_2/HF sequence at 150°C exhibited an etch per cycle of 1.38 Å, near-ideal ALE synergy of 97%, and selectivity versus Si (**Figure 3**).

11:45am **AP+EL+PS+TF-WeM-16 Controlled SiO_2 Etch Rates Using a HF/H_2O Liquid-Layer in a Vacuum Environment: Dependence on H_2O and HF Pressures**, ***Samantha Rau,*** University of Colorado at Boulder*; Antonio Rotondaro, Hanna Paddubrouskaya, Kate Abel,* Tokyo Electron America, Inc.*; Steven George,* University of Colorado at Boulder

Our earlier research demonstrated SiO_2 etching by HF using a H_2O liquid-layer in a vacuum environment. The current work characterized the dependence of SiO_2 etch rate on the H_2O and HF pressures. We have observed a dramatic increase in SiO_2 etch rates at higher H_2O and HF pressures. This behavior suggests that the thickness of the HF/H_2O liquid-layer may be increasing rapidly at higher pressures.

SiO_2 etch rates may be sensitive to the HF/H_2O liquid-layer thickness when the thickness is close to the size the hydrated F^-, HF_2^- and SiF_6^{2-} ions that are involved during SiO_2 etching. For example, the size of the hydrated F^- ion is 7 Å. Lower SiO_2 etch rates may result from incomplete hydration of these ions. SiO_2 etch rates may approach the SiO_2 etch rates observed in solution for thicker liquid-layers.

Investigations were performed to determine the thresholds for HF/H_2O condensation versus H_2O and HF pressure. Spectroscopic ellipsometry was employed to measure the liquid-layer thickness, the mean squared error (MSE) in the thickness model, and the transmitted light intensity. Condensation was assumed to occur when the increase in liquid-layer thickness, the increase in MSE, and the decrease in light intensity all occurred rapidly at higher H_2O and HF pressures. Figure 1 shows that rapid changes in the liquid-layer thickness, MSE and transmitted light intensity are observed at a total pressure of 22.9 Torr (18 Torr H_2O and 4.9 Torr HF) at 30.4°C.

Experiments were conducted at initial H_2O pressures from 0-35 Torr and increasing HF pressures from 0-40 Torr to determine the threshold H_2O and HF pressures for condensation at 30.4°C. The resulting condensation points were then compared with the measured SiO_2 etch rates at various H_2O and HF pressures in Figure 2. Below the condensation curve in the ultrathin liquid layers, there were lower SiO_2 etch rates ranging from ~1-100 Å per 5 s HF exposure. These lower SiO_2 etch rates may result from incomplete hydration of the F^-, HF_2^- and SiF_6^{2-} ions. Above the condensation line, the measured SiO_2 etch rates of ~100-1000 Å per 5 s HF exposure were comparable with SiO_2 etch rates in bulk HF solutions with HF wt% values of 25-40%.

12:00pm **AP+EL+PS+TF-WeM-17 Thermal Selective Etching of $Si_{1-x}Ge_x$ in XeF_2**, ***Daniel Cho***[1]*, Yi Chen, Harrison Cameron,* UCLA*; John Hoang, Nick Altieri, Ji Zhu, Samantha Tan,* Lam Research Corporation*; Jane P. Chang,* UCLA

In GAAFET fabrication, $Si_{1-x}Ge_x$ is etched selectively from Si. Wet, plasma, and thermal chemistries have been investigated to etch $Si_{1-x}Ge_x$ with a range of selectivity [1]. Thermal fluorine-based etch processes, including F_2 and XeF_2, show high selectivity with etch rates exhibiting a volcano-shaped dependence on x [2, 3].

In this study, we report $Si_{1-x}Ge_x$ (x = 0 to 1) etch by a XeF_2 beam. XeF_2 was sublimed into an expansion chamber to a target pressure, then pulsed into the reaction chamber. In each pulse, ΔP_{XeF2} was proportional to the XeF_2 dose. *Ex situ* x-ray photoelectron spectroscopy (XPS) identified the chemical bonding states on the $Si_{1-x}Ge_x$ surface from XeF_2, while scanning electron microscopy (SEM) measured the etch depth for etch rate (ER) calculations.

XeF_2 exposure on as-received $Si_{1-x}Ge_x$ samples showed no etch, confirmed by XPS and SEM. This was attributed to a native oxide which prevented XeF_2 from interacting with the underlying $Si_{1-x}Ge_x$. Prior to XeF_2 exposure, *in situ* Ar ion sputtering was used to remove the native oxide for all sequential etch conditions.

XPS results of XeF_2-processed $Si_{0.75}Ge_{0.25}$, Si, and Ge identified Ge-F, Si-F, and C-F bonding in the F 1s region at binding energies of 685.0 eV, 687.1 eV, and 689.6 eV, respectively, consistent with literature values [4-6]. Ge-F, Si-F, and C-F made up 20.8%, 37.4%, and 41.8% of the total fluorine content on the XeF_2-processed $Si_{0.75}Ge_{0.25}$. Quantitative analysis of fluorination by *ex situ* XPS was limited by air exposure between etch and measurement.

Synergistic etching, with Ar ions and XeF_2 simultaneously exposed, showed a Si ER of 6 nm/pulse at an ion beam voltage of 200 V and ΔP_{XeF2} =0.5 Torr, showing a higher ER than the sequential Si ER of 0.4 nm/pulse at the same ion beam voltage and ΔP_{XeF2}.

The peak sequential $Si_{1-x}Ge_x$ ERs for the following Ar ion beam voltage and ΔP_{XeF2} conditions, 100 V and 0.5 Torr, 200 V and 0.5 Torr, and 100 V and 0.2 Torr, were 7.8 nm/pulse, 9.9 nm/pulse, and 4.1 nm/pulse, respectively. For all conditions, ER increased from x = 0 to 0.1, followed by a decrease or plateau past x = 0.15. Higher pretreatment ion beam voltage and higher ΔP_{XeF2} both led to an etch rate increase for x = 0 to 0.25. The peak $Si_{1-x}Ge_x$/Si etch selectivity ranged from 20 to 30 under all conditions.

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[1] **JVST Highlighted Talk**

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