Advanced Microelectronic Materials and Devices Mini-Symposium
Room 318 - Session AM2+EM+TF-FrM
Devices II

Moderators: Samantha Jaszewski, Sandia National Labs, **Somil Rathi**, Arizona State University

10:30am **AM2+EM+TF-FrM-10 Development of Metallic Gate Stacks at Atomic Scale : Application to Advanced FD-SOI Transistors***, Elouan Le Cun, Julien Patouillard, Rémy Gassilloud, Mathieu Bernard, Zdenek Chalupa, Krunoslav Romanjek, Wissem Baik, William Vandendaele, Elhadji-Alhousseyni Diallo, Tadeu Mota Frutuoso, Pauline Hauchecorne, Virginie Loup, Théo Cabaret, Frédérique Glowacki, Mouaad Yassine Aliouat, Elise Arnoux, Gennie Garnier, Marie-Claire Cyrille, Olivier Renault, Claire Fenouillet-Béranger,* CEA-LETI, France

Fully-Depleted Silicon On Insulator (FDSOI) planar technology - an alternative to FinFET (3D field effect transistors) - address technologies involving very high energy efficiency, ultralow power consumption and cost reduction. 10 nm FD-SOI transistor requires complex metal on insulator (MOS) gate stacks. The MOS structure is composed of doped titanium nitride layers as metal gates, and SiON/HfON as gate-dielectric[1]. SiON is also called gate interlayer (IL). Thinning TiN layers results in better MOS performances. This is due to a known phenomenon called IL scavenging, where TiN acts as an oxygen reducer of the IL, which in turn reduces the IL thickness[2]. The targeted TiN thickness in the 10 nm-node FDSOI is closed to 2 nm, and the required equivalent oxide thickness (the electrical thickness of the IL/HfON insulator stack) is below 0,8 nm. As the layers thicknesses reach the nm-scale, it introduces new challenges regarding the electrical behavior of the MOSFET due to the heterogeneity of the materials in the gate stacks.

To address those challenges, the developments of an ultra-thin 2 nm metallic gate stack with sub-stoichiometric titanium nitride ($TiN_{x<1}$) are required. CEA-Leti has acquired a PVD deposition tool by co-sputtering to deposit complex metallic layers on 300 mm silicon wafers with an atomic-scale thickness control.

This study examines TiN_x ultra-thin films with thicknesses below 5 nm. TiN_x structural, optical and electrical properties are evaluated by X-Ray Reflectivity (XRR), stress measurements, sheet resistance measurements, spectroscopic ellipsometry, X-Ray Photoelectron Spectroscopy (XPS) and X-Ray Diffraction (XRD). TiN_x layer composition is investigated by Elastic Recoil Detection Analysis (ERDA) and X-Ray Fluorescence (XRF) analysis. Those layers have been integrated on simplified electrical devices to evaluate their impact on transistor key performance parameters (EOT, Vt, Jg, ...).

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References:

[1] C. Fenouillet-Beranger, et al, “Pursuing the FD-SOI roadmap down to 10 nm and 7 nm nodes for high energy efficient, low power and RF/mmWave applications,” Solid-State Electron. 231, 109264 (2026).

[2] T. Ando et al., Ultimate Scaling of High-κ Gate Dielectrics: Higher-κ or Interfacial Layer Scavenging, Materials 2012, 5, 478-500

10:45am **AM2+EM+TF-FrM-11 Towards Ordered Growth of Complex Oxide Thin Films for Memristive Devices***, Michael Mitchell*[1]*, Xianchao Dong, Shweta Joshi, Tianshu Li, Gina Adam,* George Washington University

We present progress towards the ordered growth of the entropy-stabilized oxide, $(MgNiCoCuZn)_{0.2}O$, via reactive magnetron sputtering for the fabrication of memristive devices. To produce this film, the authors leveraged a custom-designed AJA ATC system with off-axis capabilities to reduce deposited atom kinetic energy and improve film crystallinity. The proposed methodology uses co-sputtering of multiple metal alloy targets in an oxygen-rich environment. Depositions are conducted at multiple substrate temperatures to identify phase transition temperatures. In addition to 100-oriented silicon, substrates composed of materials with improved lattice matching to literature values of $(MgNiCoCuZn)_{0.2}O$ are employed, and the relationship between substrate material and phase transition temperature is investigated. Various microscopic and spectroscopic characterization techniques, including Atomic Force Microscopy (AFM) and Energy Dispersive X-ray Spectroscopy (EDS), etc., were used to determine the film growth rate and stoichiometry. Molecular Dynamics simulations, with interatomic interactions provided by fine-tunned machine learning models, are employed to study the relationship between phase transition temperature and substrate composition. The computational findings for the influence of substrate composition and deposition stoichiometry on the phase transition temperature are then compared with the experimental results. The pathways for integration of the resulting film into memristive devices are also discussed.

11:00am **AM2+EM+TF-FrM-12 Ambipolar Organic Transistor Based on Polypeptides***, Jeyvin Coleman,* University of Nebraska - Lincoln*; Mariam Orabi, Wai Kiat Chin, Peter Dowben,* University of Nebraska-Lincoln, USA

Ambipolar organic field-effect transistors have seen years of development and have been a topic of interest now for several decades. The dual-polarity allows for more simple circuit architecture for organic electronics. Generally, the performance of planar ambipolar organic transistors is poor and requires the deposition of two different organic semiconductors [1-3]. Frequently, the mobility is well below 1 $cm^2 V^{-1}s^{-1}$, usually by orders of magnitude. Here, we look at bio-organic polypeptides to reduce the fabrication steps for flexible electronics. We show that polypeptide-based materials have potential in organic electronic devices, more specifically, they are seen to make excellent organic ambipolar transistors. In this study, organic field-effect ambipolar transistors (OFETs) were fabricated using poly-D-lysine, poly-L-ornithine and poly-L-aspartic acid combined with poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS). Under ambient light, the poly-D-ornithine based devices showed higher overall on-state currents, while the poly-L-lysine-based devices exhibited significantly higher on-state currents under dark conditions, with differences of at least two orders of magnitude. Thus, we have two distinct types of bio-organic ambipolar transistor devices. Both the poly-D-lysine and poly-L-ornithine devices also demonstrated relatively long carrier lifetimes, ranging from 10^{-6} to 10^{-3} s, while the bio-organic ambipolar transistor made from poly-L-aspartic acid combined with PEDOT:PSS has a mobility of 1 $cm^2 V^{-1} s^{-1}$. Comparing the calculated and experimentally measured band-gap energies provides complementary information about the electronic structure of the polypeptide materials. Overall, these results demonstrate and highlight the potential of these polypeptide materials for organic electronic applications and highlight the potential of polypeptides as tunable materials for low-voltage bio-organic ambipolar transistors.

1. Baeg, K.-J. et al., IEEE Electron Device Lett. 34, 126–128 (2013).

2. Zhang, Z. et al., Adv. Funct. Mater. 25, 6112–6121 (2015).

3. Kraft, U. et al.,. Adv. Mater. 27, 207–214 (2015)

11:15am **AM2+EM+TF-FrM-13 Limitations of Layered Dielectrics***, Peter Dickens, Brianna Klein, Andrew Binder,* Sandia National Laboratories, USA

Next-generation power conversion systems increasingly rely on SiC power MOSFETs to minimize switching losses and maximize power density. Conventional SiO_2 gate dielectrics limits maximizing the gate capacitance and drive current, making higher-k dielectrics attractive to improve switching characteristics.However, to date, severe defect densities at the direct high-k/SiC interface has prevented strict high-k adoption.Consequently, recent work has focused on utilizing a dielectric bilayer with SiO_2 serving as the interface dielectric with SiC to enable low defect densities and a high-k stacked on top in an attempt to gain the “best of both worlds”.Despite some reported successes, there remain critical gaps discussing what fundamental advantages or limitations exist from this dielectric bilayer approach.

In this presentation, we present analysis of the available design space for layered dielectrics in SiC-based MOSFETs.Our analysis operates under three fundamental assumptions related to applied gate bias, avoidance of time-dependent-dielectric-breakdown (TDDB), and the requirement to be high-k (effective dielectric permittivity greater than the permittivity of the semiconductor).We show that when these assumptions are applied then the available design space for layered dielectrics is quite limited and calls into question advantages of a layered approach.

[1] **JVST Highlighted Talk**

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