Functional Thin Films and Surfaces
Room Town & Country D - Session C2-1-WeA

Thin Films for Electronic Devices I

Moderators: Julien Keraudy, Oerlikon Balzers, Oerlikon Surface Solution AG, Liechtenstein, **Jörg Patscheider**, Evatec AG, Switzerland

3:20pm **C2-1-WeA-5 Developing Electronic Materials With an Eye Towards Packaging**, ***Marcel A. Wall (marcel.a.wall@intel.com)***, Intel Corporation, USA **INVITED**

Heterogeneous integration of multiple types of Integrated circuit chips on a single package is an emerging area in advanced packaging that has made significant impact to High Performance Computing (HPC) devices. In this presentation, we will discuss the evolution of heterogeneous System in Package (SIP) packaging technologies. We will provide an overview of key drivers and metrics for enabling advanced die to die and on package interconnect technologies . We will cover the areas of innovation needed in materials, equipment, process and design in advancing the next generation of heterogeneous SIP packaging technologies. Finally, we will cover some of the unique requirements needed of basic thin film materials used in electronics, as it applies to packaging.

4:00pm **C2-1-WeA-7 Crystallographic Study of Non-polar $Al_{0.7}Sc_{0.3}N$(11-20) Grown on r-plane Al_2O_3 Using Magnetron Sputter Epitaxy**, ***Akash Nair (akash.nair@iaf.fraunhofer.de)***, *L. Kirste,* Fraunhofer Institute for Applied Solid State Physics IAF, Germany*; N. Manuel Feil,* University of Freiburg, Germany*; M. Prescher, A. Žukauskaitė,* Fraunhofer Institute for Applied Solid State Physics IAF, Germany

Aluminium scandium nitride (AlScN) has emerged as a promising material for fabrication of bulk acoustic wave (BAW) and surface acoustic wave (SAW) devices by virtue of its high piezoelectric properties and improved electromechanical coupling. Despite the high interest, AlScN remains relatively unexplored material in terms of the structural properties and device applications. We recently demonstrated that non-polar $Al_{0.77}Sc_{0.23}N$ offers a pathway for further improvement in electromechanical coupling for SAW resonators by aligning the acoustic wave along the c-axis direction with the largest piezoelectric response[1]. The metastable nature of $Al_{1-x}Sc_xN$ at higher scandium concentrations, that causes formation of abnormally oriented grains (AOG) protruding from surface of the films, has been a challenge for its adoption for SAW applications. We succeeded in achieving the growth of completely AOG-free non-polar in-plane oriented $Al_{1-x}Sc_xN$ films with even higher Sc content of x=0.3 by reactive magnetron sputter epitaxy. Various sputtering process conditions were investigated focusing on the $Al_{0.7}Sc_{0.3}N$(11-20)/Al_2O_3(1-102) film. Surface quality and films with RMS roughness less than 0.5 nm could be obtained. The atomic force microscopy (AFM) and x-ray diffraction (XRD) studies of films show a unique striated grain morphology along the c-axis of the film revealing in-plane anisotropy. While the XRD measurements confirm the in-plane orientation of $Al_{0.7}Sc_{0.3}N$(11-20), the φ scans also reveal a distorted wurzitic structure and structural anisotropy. The structural anisotropy is studied by combining transmission electron microscopy, high resolution XRD and AFM. Furthermore, the optimized $Al_{0.7}Sc_{0.3}N$(11-20) films were used to fabricate SAW resonator test structures. Different in-plane SAW propagation directions were used to map the angular distribution of effective electromechanical coupling as well as piezoelectric properties of non-polar AlScN thin films and correlated to the results of structural anisotropy study.

[1] A.Ding, et al., APL 116(10), 101903 (2020).

4:20pm **C2-1-WeA-8 Tuning Barrier Properties of Metal Nitride Thin Films for GaN Transistor Applications**, ***Clemens Nyffeler (clemens.nyffeler@evatecnet.com)***, *B. Attarimashalkoubeh, J. Patscheider, B. Heinz,* Evatec AG, Switzerland

Due to their thermal stability and barrier properties, conductive metal nitrides are often used in the fabrication of electronic devices, such as contact layers on the surface of a field-effect transistor's (FET) gate region. Specifically, in the case where a metal nitride layer is in direct contact with a semiconductor's surface, for example in heterojunction FETs made from III-V materials such as Gallium Nitride, the barrier function requirements are twofold. The material must prevent both, migration of metal species (diffusion barrier), and also electrical conduction into the semiconductor (Schottky barrier), thus preventing shorts between gate and channel and ensuring efficient device operation. In this context, we investigate the mentioned barrier function, electrical conductivity, and other relevant properties of thin TiN_x and WN_x layers (t < 200nm) deposited by reactive magnetron sputtering. Sputter deposition was performed on an Evatec Clusterline® 200II industrial production system for automated processing of 200mm substrates at high throughput.

Our experiments show that good barrier properties in tungsten nitride are achieved for a sub-stoichiometric, nitrogen-deficient composition of WN_x with a nitrogen content of only 20at% showing a predominant phase of (111)-oriented W_2N. For TiN_x on the other hand, we see evidence for diffusion through the barrier layer in annealing experiments for sub-stoichiometric films only. Conversely, the barrier remains effective for films deposited in a nitrogen-rich ambient, with a N2:Ar gas-flow ratio of larger than 1:1, resulting in over-stoichiometric films.

The diffusion experiments are conducted on stacks of 25nm Ti / 100nm TiN_x / 75nm Al layers (top-to-bottom, on Si substrates). Four-point probe measurements before ex-situ annealing at temperatures up to 400°C and after annealing exhibit a significant change of the measured sheet resistance. These changes are correlated to failure of the Schottky barrier function.

4:40pm **C2-1-WeA-9 Advancements in Metallic Interconnects for the Semiconductor Industry**, ***Thomas Ponnuswamy (Thomas.Ponnuswamy@lamresearch.com)***, Lam Research Corp, USA **INVITED**

The semiconductor industry is advancing from a SoC (system on ship) approach towards developing various integration schemes involving SiP (system in package) to meet the future requirements of performance and cost. This is commonly referred to as heterogeneous integration and is being utilized for 2.5D/3D chip stacking, high density fanout and chiplets. All these approaches rely on the use of metallic interconnects including TSVs (through-silicon vias), micropillars, fine line RDL, and hybrid bonding.

In the case of 3D stacking with TSVs for memory, we see an increase in the number of stacking layers and reduction of critical dimensions to accommodate higher I/O counts. The interconnects in high density fanout comprise of fine line RDL and megapillars. To meet the performance requirements line dimensions are shrinking from 5x5µm to sub 2x2µm L/S, along with incorporation of a multilayer approach. Megapillars typically range from 100 to 200µm CD with varying aspect ratios depending on the integration scheme and performance needs. Copper pillars with sub-40µm pitch are referred to as micropillars which will eventually need to be replaced by hybrid bonding as the dimensions shrink below 10µm.

Scaling requirements for each of these interconnects pose challenges that need to be addressed by making process, materials, and integration changes. In the case of TSVs, higher aspect ratios necessitate the need for alternate metallization schemes. For micropillars, increase in bump density results in challenges to assembly yield and reliability, while for fine line RDLs stress induced damage and topography control needs to be solved. Finally, in the case of hybrid bonding the key requirement of lower thermal budget for yield improvement needs to be addressed for die-to-wafer and wafer-to-wafer stacking.

This presentation will cover how select deposition processes and material changes provide solutions to the scaling challenges posed by interconnects utilized in various heterogenous integration schemes.

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