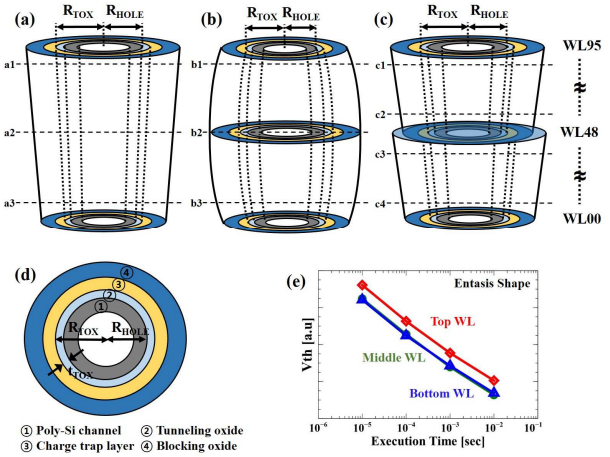

Fig. 1. Schematics of vertical GAA structure varying etching and oxidation process with (a) trapezoid, (b) entasis and (c) iterated trapezoid structures. (d) Top view for GAA in 3D CTF (e) Experimental data showing variations of erase speed along the WLs.

1st step : Modeling Structure and Fundamentals

- String-level compact modeling structure [5]
- Extraction of model parameters for FN tunneling current (using experimental data)
- Verification for variations of program/erase speed along the WLs (using experimental data)

2nd step : Process Variation and Optimizing Design

- Geometry profile such as hole radius and tunneling oxide thickness (using TCAD or measurement)
- Establishing reference WL considering device performance
- Extracting WL gate bias level for consistent electric field regardless structures

Fig. 2. Proposed workflow to obtain consistent electric field and device performance along the WLs.

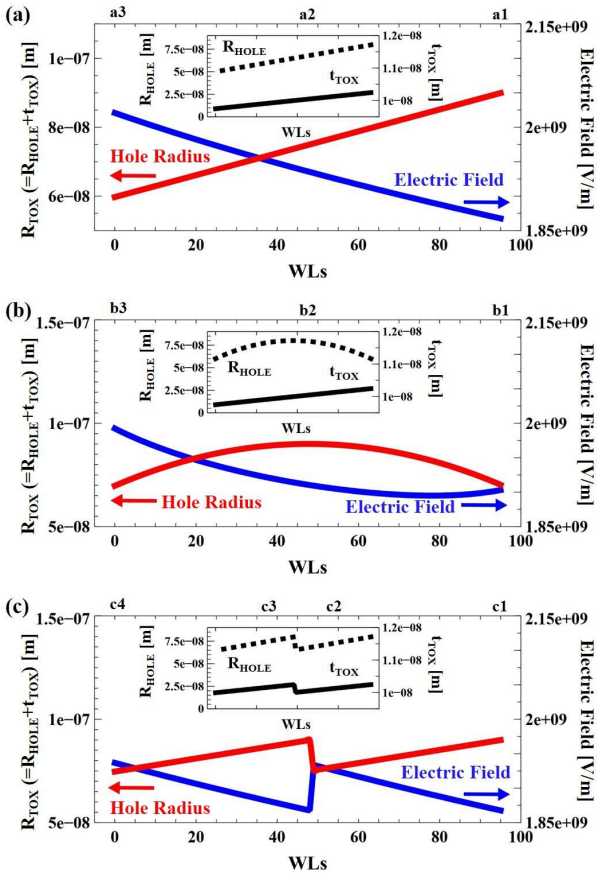

Fig. 3. Distributions for hole radius ($R_{TOX} = R_{HOLE} + t_{TOX}$) and thickness of tunneling oxide along the WLs and corresponding electric field for (a) trapezoid, (b) entasis and (c) iterated trapezoid structures. Insets of each graph show distributions of RHOLE and tTOX along the WLs.

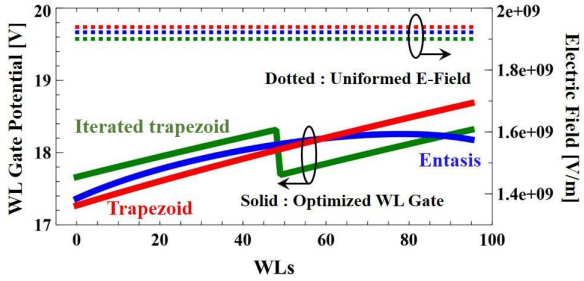

Fig. 4. Distributions for optimized WL gate biases to obtain consistent electric filed for various vertical GAA structures.

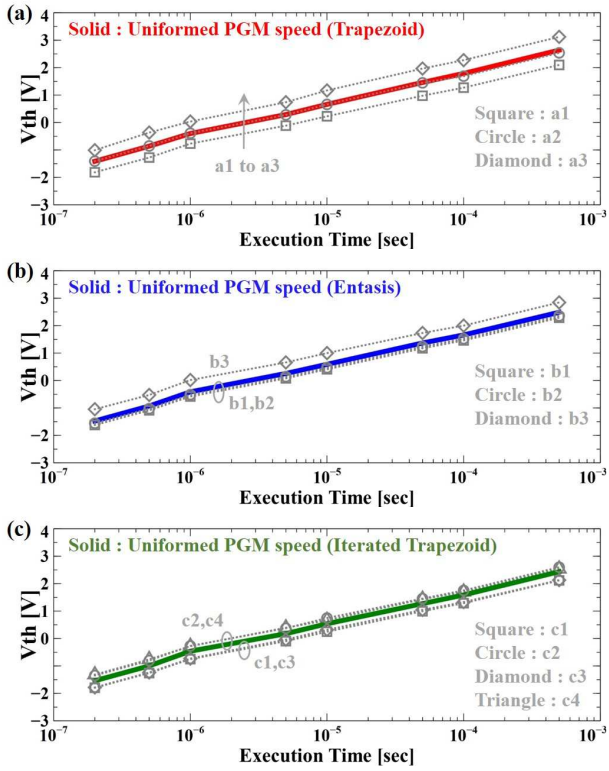

Fig. 5. SPICE simulation results for program speed at various locations within the string exhibit diverse performances, whereas the optimized results demonstrate consistent program speed, represented by solid line.