International Workshop on Gallium Oxide and Related Materials (IWGO-6)

Room ESJ 0202 - Session IWGO-FrM2

Advanced Device Scaling and Fabrication Techniques II

Moderators: Samuel Graham, University of Maryland College Park, **Marko Tadjer**, U.S. Naval Research Laboratory

10:55am **IWGO-FrM2-45 Heavy-Ion Microprobe Induced Parasitic Channel in Ga2O3 MOSFETs*, Adam Neal,*** Air Force Research Laboratory, Materials and Manufacturing Directorate, USA*; Daram Ramdin,* Core4ce*; Eric O'Quinn,* University of Tennessee Knoxville*; Adam Charnas,* Air Force Research Laboratory, Materials and Manufacturing Directorate, USA*; Kay-Obbe Voss,* GSI Helmholtzzentrum für Schwerionenforschung, Germany*; Cale Overstreet,* University of Tennessee Knoxville*; Cameron Gorsak, Hari Nair,* Cornell University*; Andrew Green,* Air Force Research Laboratory, Sensors Directorate*; Thaddeus Asel, Shin Mou,* Air Force Research Laboratory, Materials and Manufacturing Directorate, USA*; Maik Lang,* University of Tennessee Knoxville

The development of the first ultrawide-bandgap β-Ga_2O_3 transistor in 2012has spurred intensive research into material properties and device optimization for the development of advanced electronics. Space applications of β-Ga_2O_3 are of particular interest due to the established susceptibility of Si, SiC and GaN to single event-burnout effects due to heavy ion collisions. Experiments elucidating the effects of heavy-ion irradiation on β-Ga_2O_3 transistors are just beginning to be reported, and such studies are critical to inform the design and implementation of Ga_2O_3 power switches and amplifiers in space. In this study, 192 MeV ^{40}Ar and 1182 MeV Au species were used to perform spatially resolved "microprobe" characterization of Ga_2O_3 MOSFETs.Single ions are shot into the device with a lateral spatial resolution of ~0.5 micron by 0.5 micron, together with in-situ electrical characterization, to map the most sensitive regions of the device. We find that these lateral Ga_2O_3 MOSFETs do not suffer catastrophic single event burnout up to average electric fields of at least 0.66 MV/cm for 192 MeV ^{40}Ar or 0.05 MV/cm for 1182 MeV Au, but they experience significant threshold voltage shifts due to accumulated micro-dosing effects when the heavy ions impact the channel region. Analysis of I-V curves indicates a radiation-induced activation of the parasitic channel at the substrate-epi interface in these Ga_2O_3 devices causing significant negative threshold voltage shifts, where the parasitic channel was otherwise well controlled through appropriate surface treatment prior to epitaxial growth.This study points to the need for additional buffer engineering to mitigate parasitic channel formation at the substrate-epi interface for rad-hard Ga_2O_3 transistors.

11:10am **IWGO-FrM2-48 Achievement of SiO_2/β-Ga_2O_3 (001) MOS Interface with Low in Terface State Density by Employing ALD with O_3 as an Oxidant and Low-temperature (600℃) Post-deposition Annealing*, Atsushi Tamura,*** *Hayama Imaida, Koji Kita,* University of Tokyo, Japan

[Introduction] While a high-temperature (1000℃) O_2 annealing has been reported to efficiently reduce interface state density (D_{it}) in SiO_2/β-Ga_2O_3 MOS structures probably by removing oxygen deficiencies in the stack [1], it leads to serious drawbacks including the change in dopant profiles and a significant decrease in carrier density in β-Ga_2O_3 [2]. Therefore, it is essential to develop a low-temperature process to form SiO_2/β-Ga_2O_3 MOS interfaces. Taking into account of the necessity of oxygen deficiency removal as mentioned above,one of the keys is a selective oxidation of the SiO_2/β-Ga_2O_3 near-interface region. Therefore, atomic layer deposition (ALD) of SiO_2 is an attractive option because it enables us to tune the degree of oxidation in the initial stage of the film growth. In this study, we investigated the influence of oxidant supply conditions in ALD on the characteristics of SiO_2/β-Ga_2O_3 MOS interfaces with low-temperature (600℃) post-deposition annealing (PDA).

[Experimental] 11 nm-thick-SiO_2 films were deposited on n-type β-Ga_2O_3 (001) epi-wafers (N^D ~10^{16}cm^{-3}) at 300℃ via ALD using TDMAS as a precursor. The initial 3 nm of SiO_2 was deposited using either O_2-remote-plasma-ALD or thermal-ALD employing O_3 as an oxidant, followed by an additional 8 nm of plasma-ALD. In the thermal-ALD, two kinds of O_3-doses per cycle (high or low-dose controlled by changing gas supply pulse duration) were employed. After PDA at 600℃ in 0.1% O_2/N_2, Au gate electrodes were deposited.

[Results and Discussions] The sample fabricated via thermal-ALD with a high-dose of O_3 shows the minimum hysteresis width in the C-V curve among three samples. Regarding the energy distributions of D_{it}, its D_{it} is approximately one-third of that of the plasma-ALD sample, achieving approximately 1×10^{11} eV^{-1}cm^{-2} at 0.2 eV below the conduction band edge. These results indicate that a sufficient O_3 supply to promote the oxidation of the near-interface region while avoiding plasma damage would be beneficial for reducing interface defect density with PDA at 600℃. Such a beneficial influence of employing O_3 as an ALD oxidant seems consistent with our previous results on Al_2O_3/β-Ga_2O_3 stacks [3]. This abstract is partly based on results obtained from a project, JPNP22007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

[1] K. Kita et al., ECS Trans. 92, 59 (2019). [2] T. Kobayashi Appl. Phys. Lett. 126, 012108 (2025). [3] A. Tamura et al., Int. Workshop on Dielectric This Films for Future Electron Dev. 2025, Sendai, Japan.

11:40am **IWGO-FrM2-54 High-Performance β-Ga_2O_3 Vertical Diodes and FinFETs with High Electric Field Strength*, Sriram Krishnamoorthy,*** University of California at Santa Barbara **INVITED**

β-Ga_2O_3 holds immense potential for power device applications in the medium to high voltage regime, for power conversion using solid state transformers in AI data centers. **Trench Diodes:** We report on vertical Schottky barrier diodes (SBDs) based on β-Ga2O3 with trench architecture, featuring a high-permittivity dielectric RESURF structure. The incorporation of a trench geometry, coupled with the high-permittivity dielectric RESURF, effectively reduces the surface electric field at the metal-semiconductor junction. This reduction facilitates the use of a lower work-function anode contact, further diminishing the turn-on voltage. The combination of lower stored charge and a low forward voltage drop results in an excellent trade-off between conduction and switching power loss, yielding a QCVF figure of merit comparable to commercial bare die SiC SBDs. **Heterojunction Diodes:** Integration of p-type oxides with Gallium Oxide offer a way to circumvent the lack of p-type Gallium Oxide to increase built-in potential of junctions with lightly doped Gallium Oxide drift layers. We report on > 3 kV NiO and Cr_2O_3 heterojunction diodes with promising performance. > 1 A devices can be realized and double pulse testing of high current diodes with record low reverse recovery charge and time indicate the promise of topology. **Vertical Transistors:** A β-Ga_2O_3-based multi-fin vertical FinFET featuring a thick field oxide layer at the trench bottom to enhance the breakdown voltage will be discussed. With novel edge termination, we report a vertical FinFET with strategies to reduce electric field crowding around device edges, leading to enhanced breakdown voltages. To reduce the gate capacitance for superior switching performance, vertical FinFETs with split gate design are also fabricated. The devices are fabricated on (001) β-Ga_2O_3 HVPE epilayers grown on Sn-doped substrates. This approach of utilizing a vertical FinFET with split gate presents a promising solution for vertical power switches with enhanced breakdown capabilities and better switching performance. Using high voltage C-V measurements the drift layer thickness was extracted to be 11 µm, resulting in a record high average electric field of 3.1 MV/cm for the 3.4 kV FET, which is the *highest reported average electric field (V_{BR}/t_{drift}) in any vertical power transistor*, 3X the average fields in GaN and SiC vertical power transistors. Further improvements in β-Ga_2O_3 material and oxide quality will significantly enhance the performance of such devices with effective electric field management and edge termination.

12:05pm **IWGO-FrM2-59 Diffusion Suppression of Mg and High Performance β-Ga_2O_3 Current Blocking Layers by N+Mg Co-Doping Approach*, Fenfen Fenda Florena,*** *Hironobu Miyamoto, Yuki Koishikawa, Hirofumi Shinohara, Kohei Sasaki, Akito Kuramata,* NCT, Japan

Deep acceptor doping is a promising strategy for forming current-blocking layers (CBLs) in β-Ga_2O_3 vertical power devices, where p-type doping is not feasible. By compensating donor concentrations, deep acceptors create high-resistivity regions that mimic p-type body layers. While single Mg or N implantation has been demonstrated for CBL formation, these approaches suffer from high leakage current and premature breakdown. In Mg-implanted CBLs, profile distortion due to Mg diffusion during high-temperature post-implantation annealing (PIA) limits performance. To overcome these limitations, a co-doping approach have been explored theoretically to induce shallow acceptor levels via donor-acceptor level repulsion effect. This work presents the first experimental demonstration of N+Mg co-doping in β-Ga_2O_3 achieving improved CBL performance.

Multi-energy N and Mg implantations were introduced into β-Ga_2O_3 to form CBL, followed by PIA. Figure 1 shows the depth profile of N and Mg as revealed by secondary ion mass spectrometry (SIMS) measurement. At 1/1 depth ratio of N/Mg, alteration of Mg profile was detected due to massive Mg diffusion toward epilayer/substrate interface. Impressively, a

remarkable Mg profile stability was achieved by implanting N much deeper into region (N/Mg = 2/1). Suppression of leakage current was more prominent in N+Mg co-implanted CBL compared to its single counterpart (more than two orders of magnitude) as shown in Fig. 2. Moreover, higher N/Mg depth ratio led to increase in breakdown voltage from 2.0 kV to 2.5 kV. This paper is based on results obtained from a project, JPNP22007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO).

12:20pm **IWGO-FrM2-62 >3.3 kV Ga_2O_3 Monolithic Bidirectional Switch: Impact of NiO/Ga2O3 Interface Charges**, *Yuan Qin,* Virginia Tech*; **Yuhao Zhang,*** The University of Hong Kong, China

Bidirectional switches (BDSs), which block bipolar voltages in the off-state and conduct current in both directions in the on-state, are essential for AC power electronics [1]. Monolithic BDSs (MBDSs) with a shared drift region can reduce device area by about four times compared with solutions based on two discrete devices [2]. With its high critical electric field and superior thermal stability, ultra-wide-bandgap Ga_2O_3 is promising for high-voltage power devices, making it attractive for high-voltage power device applications. After earlier demonstrations of low-voltage Ga_2O_3 MBDSs [3], [4], we recently reported a JFET-based Ga_2O_3 MBDS with BV over 6.5 kV in both polarities [5]. However, its on-resistance (R_{on}) is still much higher than the ideal value predicted from channel resistivity analysis, and its reliability remains unclear.

This work investigates the R_{on} and reliability of a Ga_2O_3 MBDS, with a particular focus on the influence of NiO/Ga_2O_3 interface charges. The elevated R_{on} originates from the non-uniform current distribution caused by the NiO junction termination extension (JTE) and interfacial charges. Negative charges at the NiO/Ga_2O_3 interface are identified as the main factor responsible for the increased R_{on}. To assess the impact of these interface charges on long-term device reliability, reverse-bias stress tests at 3.3 kV were conducted. The minimal parametric drifts observed suggest that these interface charges correspond to deep-level traps and do not substantially affect the device's long-term performance. These findings offer valuable insights and guidelines for further optimizing the figure of merit of high-voltage lateral Ga_2O_3 devices.

[1] B. J. Baliga,IEEE Power Electron. Mag. **10**, 20(2023). [2] Y. Guo, IEEE Electron Device Lett. **46**, 556(2025). [3] P. Sharma, Appl. Phys. Lett. **125**, 253502(2024). [4] D. Chettri, Appl. Phys. Lett. **125**, 202104(2024). [5] Y. Qin, IEEE Electron Device Lett. **47**, 245(2026).

12:35pm **IWGO-FrM2-65 Kilovolt Class β-Ga_2O_3 Split Gate Vertical FinFET for Reduced Gate Capacitance**, ***Saurav Roy,*** North Carolina State University*; Chinmoy N. Saha, Yizheng Liu, Akhila Mattapalli, Carl Peterson, James S. Speck, Sriram Krishnamoorthy,* University of California Santa Barbara

The first vertical FinFETs using β-Ga_2O_3 were reported by Hu et al. [1], followed by the demonstration of multi-fin vertical FinFETs by Li et al. [2]. A β-Ga_2O_3-based multi-fin vertical FinFET featuring a thick field oxide layer at the trench bottom to enhance the breakdown voltage is reported in [3]. However, the edge of the device periphery remains the location, where electric field crowding happens and as a result leads to premature breakdown. In this work we report a vertical FinFET with an edge dielectric to reduce electric field crowding around device edges. To reduce the gate capacitance for superior switching performance, vertical FinFETs with split gate design are also fabricated.

The devices are fabricated on (001) β-Ga_2O_3 HVPE epilayers grown on Sn-doped substrates. Si ion implantation was performed on the top surface. The fins, 200 nm in width, were defined using electron beam lithography to ensure normally-off operation. These fins were etched using BCl_3 plasma, achieving a height of 1.2 µm. After fin definition, a 150 nm PECVD SiO_2 was deposited as the field oxide. The oxides from the sidewalls and top of the fins were then removed through a self-aligned planarization process followed by wet etching. SiO_2 is then sputter deposited around the device periphery as first edge dielectric A 30 nm layer of Al_2O_3 was deposited as the gate oxide using atomic layer deposition (ALD). Mo was then sputtered as the gate contact and etched to establish source-gate isolation via photoresist planarization. For split gate device, the Mo etch is performed to etch the gate metal from the trench region. A second edge dielectric layer is then deposited using sputtering around the device periphery. An SiO_2 spacer layer was then deposited to isolate the gate and source contacts. Finally, Ti/Au source and drain pad contacts were deposited on the front and back of the sample using e-beam evaporation.

The transfer characteristics of the fabricated vertical FinFETs without and with split gate, displayed in both linear and logarithmic scales demonstrates an on-off ratio of ~10^{10} for both FinFETs without and with split gate. A threshold voltage of 0.8 V is observed. The output characteristics of the fabricated FinFETs without and with split gate shows a specific on-resistance of 18 mΩ-cm^2 and 37 mΩ-cm^2 respectively. The current densities are normalized using the entire source contact area. Three-terminal off-state breakdown measurements reveal a breakdown voltage of 3.4 kV for the vertical FinFET without the split gate and 2.7 kV with the split gate. The capacitance measurement performed on the device shows lower C_{GS} and C_{GD} for the split gate devices.

12:50pm **IWGO-FrM2-68 Closing Remarks**

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