Buffer layer growth for III-V on Si substrates using Molecular Beam Epitaxy

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As we approach the physical limits of silicon in the semiconductor industry, there have been many attempts to overcome these obstacles. One of these attempts is to use III-V semiconductors due to its superior physical characteristics. However, epitaxial growth of III-V materials have been limited to III-V substrates such as GaAs and InP. In order to take advantage of Si substrates, which has been used for decades in the semiconductor industry due to its ease of use, low cost, availability in large areas and physical properties such as thermal conductivity, a well-constructed buffer layer is critical for heteroepitaxy of III-V materials. This buffer layer may overcome defects such as threading dislocation and anti-phase boundaries which are normally associated with heteroepitaxial growth. Here, we demonstrate the growth of a buffer layer using a seed layer and SPS to minimize defects.

Fig. 1(a) shows the structure of III-V on Si using a seed layer and Short-Period Superlattice (SPS). The AlAs seed layer is grown at a high temperature while the AlAs/GaAs SPS is grown at a low temperature. The buffer layer is terminated by an InGaAs/GaAs Defect Fiter Layer (DFL) structure. The surface roughness measured by Atomic Force Microscopy (AFM) was 2 nm (root mean square) (Fig. 1(b)). Fig. 1(c) shows the cross-section of the buffer layer using Transmission Electron Microscopy (TEM). It is apparent that the surface is improved in AlAs/GaAs SPS and the dislocation is decreased InGaAs/GaAs DFL. Fig. 1(d) shows the result of Etch-Pit Density (EPD) measurement using KOH solution and Optical Microscopy (OM). Average EPD value was 3,000 /cm^2. As a result, we expect to grow low-cost, high-efficiency devices by growing III-V compound semiconductor on Si substrates.

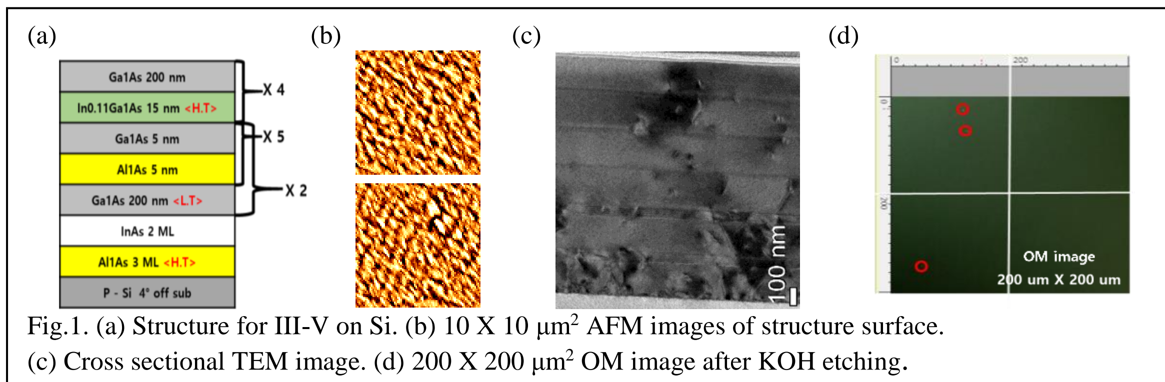

Fig.1. (a) Structure for III-V on Si. (b) 10 X 10 μm^2 AFM images of structure surface. (c) Cross sectional TEM image. (d) 200 X 200 μm^2 OM image after KOH etching.

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