III-V Transistors for nm Logic and 100-1000 GHz Wireless

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We examine the opportunities for nm III-V electron devices both in VLSI logic and in mm-wave (and sub-mm-wave) wireless communications.

Tunnel FETs (TFETs) are being developed for high on-off current ratios at low operating voltages, enabling low-power VLSI. III-V heterojunction TFETs offer direct (vs. phonon-assisted) tunneling, low tunnel barrier energy, and low electron effective mass. TFET on-currents are nevertheless very low; consequently TFET logic will be very slow. We are developing modified (triple-heterojunction) TFETs [1]. In these, added wide-bandgap source and channel layers increase the junction built-in potential, increasing the junction field and thereby decreasing the tunneling distance. $[1\bar{1}0]$ confinement with $[110]$ transport decreases the hole mass. The tunneling probability is greatly increased, proportionally increasing the on-current and logic speed. As the heterojunctions must be perpendicular to the semiconductor-dielectric interface, both convention TFETs are profoundly difficult to fabricate. Addressing this, our fabrication process, which we are developing, uses template assisted selective epitaxy [2].

Wireless communications will soon move to 5G (28, 38, 57-71, 71-86GHz); research now explores 100-1000 GHz systems. Above ~200GHz, CMOS provides little or no amplification, and scaling below ~32nm does not improve this. We must develop transistors for the low-noise and high-power stages in 100-200GHz systems, and for all stages at higher frequencies. InP HBTs, useful for power, have reached 1.1THz f_{max}. To further improve bandwidth, we are exploring TESA processes to form devices with buried dielectric layers in the base-collector junction. The base contact can be made wider for reduced resistance while the buried dielectric layer maintains low junction capacitance. InP HEMTs, useful for noise, have reached 1.5THz f_{max}. To further improve bandwidth, we are developing nm InAs MOS-HEMTs, with ALD ZrO_2 gate dielectrics, 5nm channels, and modulation-doped access regions surrounding the gate.

[1] P. Long, *et al*., 2017 Device Research Conference, June, Notre Dame.
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