III-V Nanowire Devices: A 3D Toolbox with Contact, Interface, and Heterostructure Engineering

Lars-Erik Wernersson
Dept. Electrical and Information Technology, Lund University, Sweden

III-V nanowires are attractive for device applications. The small nanowire footprint reduces the number of propagating defects opening a path for integration of high-quality III-V materials on Si. The direct band gap and the wide range of wave lengths addressable makes the material suitable for optoelectronic applications including light emitting diodes, solar cells, and long wave length photodetectors. The advantageous transport properties find usage in transistors applications where the reduced scattering enhances the drive current. However, for the realization of these devices, processing strategies needs to be developed and the material carefully characterized to avoid detrimental parasitic effects on the device performance.

In this talk, III-V nanowire MOSFETs [1] and TunnelFETs [2] will be presented. State-of-the-art performance in terms of transconductance (g_m), drive current (I_{on}), subthreshold swing (S), and off-state leakage current (I_{off}) will be demonstrated. In particular, we will focus on InAs/InGaAs MOSFETs and InAs/InGaAsSb/GaSb TunnelFETs, where the nanowire growth technology allows for incorporation of materials with strong lattice mismatch into the transistor channel.

The transistor processing relies on understanding and control of the physics and chemistry at the transistor interfaces. Examples will be given including vertical TLM structures developed to evaluate the specific contact resistance [3]. Furthermore, a vertical gate-last process has been established to align the gate to the edges of the source and drain contact regions reducing access resistance [4]. The semiconductor/high-*k* interface has finally been evaluated and the growth and process technology optimized to reduce both interface state and border trap state densities [5].

[1] O.-P. Kilpi, et al Vertical InAs/InGaAs Heterostructure Metal–Oxide–Semiconductor Field-Effect Transistors on Si Nano Lett., (2017)
[2] E. Memisevic, et al, Individual Defects in InAs/InGaAsSb/GaSb Nanowire Tunnel Field Effect Transistors Operating below 60 mV/decade Nano Lett., 17, 4373 (2017)
[3] M. Berg, et al A transmission line method for evaluation of vertical InAs nanowire contacts Appl. Phys. Lett. 107, 232102 (2015)
[4] M. Berg, et al, Electrical Characterization and Modeling of Gate-Last Vertical InAs Nanowire MOSFETs on Si IEEE Electron Dev. Lett., 37, 966 (2016)
[5] J. Wu, et al Low Trap Density in InAs/High-k Nanowire Gate Stacks with Optimized Growth and Doping Conditions Nano Lett., 16, 2418 (2016)