PCSI

Room Redondo - Session PCSI-TuM2

Materials for High Power Electronics

Moderator: Gordon Schmidt, Otto-von-Guericke-University Magdeburg, Germany

10:40am **PCSI-TuM2-27 Challenges in SiO_2/Si Interface Engineering for SiC Power MOSFETs**, ***Takuji Hosoi,*** Kwansei Gakuin University, Japan; *T. Shimura, H. Watanabe,* Osaka University, Japan **INVITED**

High on-resistance due to low channel mobility and threshold voltage instability due to charge trapping are major concerns of SiC-based power MOSFET, and both issues are deeply correlated with poor SiO_2/SiC interface property grown by thermal oxidation. One of the main causes of this severe interface degradation is residual carbon impurity remained near SiO_2/SiC interface. Although the most common technique to improve SiO_2/SiC interface quality is N incorporation into SiO_2/SiC interface by post-oxidation annealing in NO (NO-POA), the effect on mobility improvement is limited [1] and enhanced hole trapping is pointed out [2]. In this talk, we review the scheme of thermal oxidation and control of N atom profile to improve performance and reliability of SiC MOSFETs based on our recent results.

We demonstrated ultrahigh-temperature oxidation at low oxygen partial pressure to enhance C ejection from SiO_2/SiC interface during thermal oxidation [3]. Passive/active oxidation boundary for 4H-SiC(0001) surface was found to be at around 1600°C under 0.3% O_2/Ar ambient. In SiC MOS capacitors, nearly ideal C-V curve can be obtained by ultrahigh-temperature oxidation, while large hysteresis and positive flatband voltage shift were observed for conventional oxidation. The field-effect mobility of nMOSFET increased from 3 to about 10 cm^2/Vs by performing ultrahigh-temperature oxidation. The reduction in C-related defects was confirmed by electron-spin-resonance (ESR) spectroscopy [4]. We also found that SiC can be oxidized to form SiO_2 under CO_2 ambient at ultrahigh temperatures [5]. Furthermore, a combination of NO-POA and subsequent CO_2 annealing at moderate temperature is effective in obtaining high-channel mobility and stable threshold voltage thanks to the selective removal of N atoms on SiO_2 side at SiO_2/SiC interface and compensation of oxygen vacancies [6].

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11:20am **PCSI-TuM2-35 Epitaxial Growth of Ga_2O_3 Films with Different Ligand Structures by Mist Chemical Vapor Deposition**, ***Jang Hyeok Park****, Y. Rim,* Sejong University, Republic of Korea

Recently, gallium oxide (Ga_2O_3) has been receiving attentions for the next generation power semiconductors such as electric vehicles, solar inverters, and energy storage devices because of having a wide band gap of 5.3eV. In particular, beta phase gallium oxide is thermally stable and is formed as a large and single crystal wafer. In order to form epitaxial β-Ga_2O_3 films, hydride vapor phase epitaxy, metal organic chemical vapor deposition, pulsed laser deposition, molecular beam epitaxy, and mist chemical vapor deposition (mist-CVD) have been proposed. Among them, mist-CVD can easily control the chemical compositions and phases as well as do low cost deposition due to simple equipment without vacuum systems.

Here, we studied the effect of precursor ligand types (Ga(acac)$_3$, $GaBr_3$, GaI_3) and growth temperatures (400℃ - 700℃) on heteroepitaxial Ga_2O_3 films on the (0001) sapphire substrates using mist-CVD method.

We confirmed that crystallinity and phases strongly depended on precursor ligands and temperatures. Through the x-ray diffraction, we analyzed the crystal structures of Ga_2O_3 films. At 400℃ and 500℃ temperatures, the (0006) α-phase was observed in Ga_2O_3 films and the optimal phase of α-Ga_2O_3 films was grown by Ga(acac)$_3$. At 600℃ temperature, the (0004) ε-phase was observed in Ga_2O_3 films and the optimal phase of ε-Ga_2O_3 was grown by GaI_3. At 700℃ temperature, the (-402) β-phase was observed in Ga_2O_3 films and the optimal phase of β-Ga_2O_3 was grown by GaI_3. The images of electron backscattering diffraction showed that the crystallinity of Ga_2O_3 grown by precursor ligand types is the single crystal epitaxial growth.

As a result, we confirmed that a carbon free xxx precursor was a good candidate to form high quality β-Ga_2O_3 epitaxial films and it would be useful to understand the epitaxial growth of metal oxide semiconductors using a mist-CVD method.

11:25am **PCSI-TuM2-36 Investigating SiC/Graphene/SiC(0001) Remote Epitaxy Using Hot-wall CVD**, ***Daniel Pennachio,*** US Naval Research Laboratory; *J. Hajzus,* ASEE Research Associate at the US Naval Research Laboratory; *A. Lang,* US Naval Research Laboratory; *R. Stroud,* Former: US Naval Research Laboratory, Current: SESE, Arizona State University; *R. Myers-Ward,* US Naval Research Laboratory

Remote epitaxy (RE) is a promising new technique for epitaxial film removal and substrate reuse that utilizes monolayer graphene as a release layer [1]. Graphene grown directly on SiC(0001) substrates through Si sublimation or through propane chemical vapor deposition (CVD) is an ideal platform for remote epitaxy of wide bandgap (WBG) semiconductors as there is no need for a graphene transfer step, reducing the risk of introducing contamination or defects that can complicate the study of the remote epitaxy process. In addition, this materials system is compatible with commercially-viable WBG semiconductor growth and processing. However, SiC CVD growth is typically conducted using high-temperature hydrogen-based chemistries that could damage or remove graphene. This study investigates the effect of alternate CVD growth conditions on SiC/graphene/SiC(0001) remote epitaxy and optimizes CVD parameters to produce high-quality SiC epilayers while reducing damage to the graphene barrier. In addition, since the effect of epitaxial graphene features such as SiC macrostep morphology and associated layer inhomogeneity on the RE process is currently unknown, graphene preparation and associated morphology are varied to explore its effect on SiC epilayer formation.

Semi-insulating nominally on-axis 6H-SiC(0001) and n-type 4° off-axis 4H-SiC(0001) substrates were used to produce different SiC surface morphologies and graphene layer numbers. Ar:H_2 process gas flow ratio, growth precursor C/Si ratio, and growth temperature were optimized during hot-wall CVD RE to promote smooth film morphology. Nomarski optical microscopy, scanning electron microscopy, and atomic force microscopy found CVD deposition at 1620°C with Ar/H_2 ratios $<20/5$ slm, and C/Si ratios <1.55 to have the smoothest surface morphology and fewest polytype inclusions. Substrates with offcuts <0.1° from SiC(0001) exhibited lower epilayer macrostep density, but showed evidence of polytype impurities and 3D growth at C/Si ratios > 1.0. Point defect density in RE SiC epilayers using a graphene interface was shown to be lower than SiC homoepitaxy using similar conditions without graphene. Cross-sectional transmission electron microscopy was utilized to assess the growth interface and graphene layer integrity after CVD growth. Through this study, optimal RE growth processes are suggested for a balance of graphene survivability and SiC film morphology.

[1] Kim, Y., Cruz, S., Lee, K. et al. Nature 544, 340–343 (2017).

11:30am **PCSI-TuM2-37 Investigating the Structurally and Chemically Heterogeneous Interface of AlGaN on (111) TaC**, *D. Roberts,* National Renewable Energy Laboratory; *M. Miller,* Colorado School of Mines, USA; *A. Rice,* ***M. Brooks Tellekamp,*** National Renewable Energy Laboratory

The lack of lattice matched substrates for AlGaN is the primary limitation to achieving high-performance power electronics, high-frequency electronics, and deep UV (DUV) LEDs. This substrate limitation affects both material quality, through the formation of misfit-induced threading dislocations and strain-induced phase separation, and limitations to device geometry due to resistive or insulating electrical behavior. Dislocations and phase separation prevent AlGaN from reaching its full materials potential, and in the case of semiconducting substrates the primary loss mechanism in a vertically conductive device is resistive loss in the substrate itself. Thus, AlGaN alloys coulddrive disruptive technology iflong-standing substrate issues can be solved [1]. For $Al_xGa_{1-x}N$ there are competing effects of increasing alloy scattering, increased bandgap with increasing Al fraction, and decreasing dopant activation such that ideal compositions for power devices fall in the range $0.3 < x < 0.85$ [2]. For these compositions pseudomorphic growth on GaN and AlN is very difficult or impossible.

Recently we have reported the design of virtual substrates for $Al_xGa_{1-x}N$epitaxy consisting of (111) TaC_x grown on sapphire substrates via RF sputtering [3]. The crystallinity is subsequently improved by face-to-face annealing. These substrates offer several opportunities to improve power

electronic devices through lattice and thermal conductivity matching, high electrical conductivity, high stability, and epitaxial liftoff.

In this talk we will discuss the nucleation of AlGaN on TaC templates as performed by molecular beam epitaxy (MBE). Annealed TaC substrates show streaky-smooth reflection high-energy electron diffraction (RHEED) patterns and 6-fold rotational symmetry. The epilayers consist of $Al_xGa_{1-x}N$ in the range $0.7 < x < 1$. Using RHEED, X-ray diffraction, atomic force microscopy, and transmission electron microscopy we investigate the impact of nucleating conditions on the structure of the film and interface. During metal-rich growth we observe incommensurate RHEED features associated with laterally contracted bilayers of metal which are not observed in nitrogen-rich growth. For $Al_{0.7}Ga_{0.3}N$ we observe relaxed growth on TaC and strained growth on co-loaded AlN templates, and corresponding to this relaxed growth only the film on TaC exhibits a step-terrace structure in AFM observed as spiral hillocks.

11:35am **PCSI-TuM2-38 Tailoring Growth Interfaces of Virtual Substrates for Power Electronics**, ***Dennice Roberts**, M. Miller, A. Norman, B. Tellekamp,* National Renewable Energy Laboratory

Power electronics materials are poised to play a critical role in fulfilling next generation energy needs, with up to 90% of future energy demand predicted to flow through power electronics at some point.[1] Among a number of candidate materials, AlxGa1-xN is the strongest, having bipolar dopability, thermal and chemical stability, an ultra-wide bandgap, and demonstrated experimental feasibility. However, AlGaN growth is limited by a lack of lattice-matched substrates, ultimately stunting material quality at higher thicknesses needed for power electronics applications. Further, high power applications increasingly call for fully vertical device structures, necessitating a conductive substrate. [1] Recently our group identified the (111) plane of TaC as a conductive surface lattice-matched to $Al_{0.55}Ga_{0.45}N$, taking inspiration from prior work of AlN and GaN binaries on carbide and boride substrates. [2,3,4]

In this talk we demonstrate the growth of (111)-oriented TaC by RF sputtering. We investigate the interface of TaC with sapphire and SiC substrates and identify means to suppress competing Ta_2C nucleation in order to stabilize (111)-oriented TaC. Potential stacking sequences are identified with respect to crystal structure and observed twinning in the TaC films. We next assess structural changes and film recrystallization that results from face-to-face annealing of TaC thin films at high temperatures above 1500 ºC. Changes to grain structure and domain size are assessed by x-ray diffraction and surface morphology is explored using atomic force microscopy. **Fig 1** shows significant improvements to in- and out-of-plane strain following annealing along with the formation of terraced step edges at the film surface. Strain as a function of material composition and thickness is considered, as this may play a major role in future nucleation of AlGaN layers.

References

[1] R. J. Kaplar et al 2017, *ECS J. Solid State Sci. Technol.* 6 Q3061

[2] D. M. Roberts et al 2022, https://arxiv.org/abs/2208.11769

[3] T. Aizawa et al 2008, *J Crys Growth* 310, 1 22

[4] R. Liu et al 2002, *Appl. Phys. Lett.* 81, 3182-3184

11:40am **PCSI-TuM2-39 Titanium Dioxide Gate Dielectrics for ScAlN Barrier HEMT Structures**, ***Neeraj Nepal**, V. Wheeler, B. Downey, M. Hardy, D. Meyer,* U.S. Naval Research Laboratory

There has been increased interest in ScAlN-barrier high electron mobility transistors (HEMTs) as ScAlN has larger spontaneous and piezoelectric polarization fields than those in GaN and AlN, which can lead to larger two dimensional electron gas (2DEG) densities. Also, ScAlN with 18% Sc content is nearly latticed matched with GaN and has bandgap of 5.65 eV. Thus, ScAlN can provide a strain-free barrier for GaN HEMT structures with high carrier concentration. Recently, we have demonstrated ScAlN-barrier GaN HEMT structures with electron mobility of 910 cm^2/V-s and 2DEG density >$3x10^{13}$ cm^{-2} [1]. However, these ScAlN/GaN HEMT devices still suffer from high leakage current [2]. Integrating gate dielectrics into these novel ScAlN-barrier HEMTs is necessary to decrease the leakage current, maintain high electric field breakdown and mitigate dc-RF dispersion in order to realize the full potential of these devices.

In this talk we report growth optimization and electrical properties of atomic layer deposition (ALD) grown TiO_2 gate dielectric on ScAlN-barrier HEMTs using Ultratech Fiji Gen2 ALD reactor. ALD process windows were initially monitored and optimized on Si substrates using *in-situ* ellipsometry. Films were deposited using tetrakis(dimethylamino)titanium (TDMAT) and an Ar/O_2 plasma at 300W. The TDMAT precursor temperature was maintained at 75 ^oC, while the pulse duration was varied from 0.25 to 0.35 sec. The plasma gas chemistry was also optimized. Optimal deposition parameters were used as initial condition to further optimize ALD conditions on ScAlN surface. On ScAlN barrier HEMT structures, deposition temperature was varied from 150 to 350 ^oC.

Atomic force microscopy was measured before and after ALD deposition showing minimal change in roughness as a result of the TiO_2 deposition.Contactless resistivity measurements performed before and after ALD and were also consistent, indicating that no plasma induced damage was occurring during ALD gate deposition. Vertical current-voltage and capacitance-voltage measurements were made on a Schottky-contacted HEMT structure and compared to devices with TiO_2 gate dielectrics deposited at different temperatures to discern the full electrical impact. As an example, an extracted dielectric constant of TiO_2 layer deposited at 200°C with O_2 flow of 20 sccm was 50 with no significant change in 2DEG density (changed from $2.7x10^{13}$ cm^{-2} to $2.6x10^{13}$ cm^{-2}after TiO_2 layer). Finally, we will present the band alignment of an optimum ALD TiO_2 on ScAlN structure using x-ray photoelectron spectroscopy.

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1. Hardy et al., *Appl. Phys. Lett.***110**, 162104 (2017).
2. Green *et al*., *IEEE Electron Device Letters***40**, 1056 (2019).

11:45am **PCSI-TuM2-40 Effect of Substrate and Growth Method on Vanadium Dioxide Thin Films by RF Magnetron Sputtering**, ***Adam Christensen**, A. Posadas, A. Demkov,* The University of Texas at Austin*; B. Zutter, P. Finnegan, S. Bhullar, S. Bishop, A. Talin,* Sandia National Laboratories

Interest in vanadium dioxide (VO_2) comes from its ability to undergo a metal-to-insulator transition (MIT) from monoclinic, semiconducting M1 phase to the metallic, rutile R phase. This transition occurs at a temperature of 340 K [2] and is generally characterized by a rapid change in electrical conductivity. This makes VO_2 attractive for many electronic and optical switching applications [1,3-4].Research on VO_2 thin film deposition has run the gamut in terms of the substrates and deposition methods used, but the use of bulk yttria-stabilized zirconia (YSZ) substrates and RF sputtering in combination or CMOS compatible fabrication has not been emphasized.

In this talk, we demonstrate that the growth of VO_2 (M1) thin films and the magnitude of the MIT (on/off ratio) are strongly impacted by choice of substrate and deposition method, and these choices are not trivial. This is achieved by comparing reactive RF sputtering deposition and oxidation of a polycrystalline vanadium metal film sputtered on (100)- and (111)-oriented YSZ substrates. The dioxide stoichiometry of these films is confirmed by x-ray photoelectron spectroscopy (XPS) and Raman spectroscopy. X-ray diffraction (XRD) reveals that direct reactive sputtering on both substrate orientations yields VO_2 (B), a metastable phase epitaxially stabilized by lattice matching. The metal sputtering and subsequent oxidation process (Fig. 1a) on (100)-oriented YSZ results in (010)-oriented VO_2 (M1) exhibiting an MIT on the order of 10^3confirmed by temperature dependent conductance measurements (Fig. 1b) in CMOS compatible devices. With the same metal sputtering and subsequent oxidation process on (111)-oriented YSZ, we achieve slightly overoxidized films with similar magnitude of MIT.

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