PCSI
Room Redondo - Session PCSI-MoM2
Semiconductor Heterostructures/Nanostructures/Interfaces/Surfaces

Moderator: Norbert Esser, TU Berlin and Leibniz-Institut für Analytische Wissenschaten-ISAS-e.V.

10:40am **PCSI-MoM2-27 UPGRADED: Hydrogen Cleaning Induced Surface Modifications of GaAs(110)***, **Dorothee Sophie Rosenzweig,*** Technische Universität Berlin, Germany*; M. Hansemann,* Paul Drude Institut Paul Drude Institut für Festkörperelektronik, Germany*; P. Ebert, M. Schnedler,* Peter Gruenberg Institut Forschungszentrum Juelich, Germany*; M. Daehne,* Technische Universität Berlin, Germany*; H. Eisele,* Otto-von-Guericke-Universität, Germany

Zincblende III/V nanowires typically exhibit non-polar (110) surfaces as side facets [1]. Since characterization is mostly performed in a different (UHV)-chamber than growth, such nanowires are commonly exposed to the atmosphere. For the nanoscopic analysis of such III/V nanowire (110) growth surfaces, hydrogen cleaning is a commonly used procedure to remove residual adsorbates, such as e.g., oxygen. While hydrogen cleaning is reported to be destruction free [2] and to achieve clean, atomically flat surfaces with well-defined electronic properties—as they are expected directly after growth—the actual processes and dynamics during cleaning are rarely examined. However, a detailed understanding of these issues is crucial for the interpretation of electronic surface properties, of the growth of nanowires, as well as the incorporationand distribution of dopant atoms.

Here, we investigate the modifications of *n*-type GaAs(110) surfaces as a model system upon controlled atomic hydrogen exposure at room temperature and under commonly used cleaning conditions at the atomic level. For depiction and measurement at the atomic scale, we used scanning tunneling microscopy and spectroscopy under UHV conditions. Using these methods, we study the geometric arrangement of the adsorbed atoms, the newly introduced defects, as well as additional electronic (defect) states and Fermi level pinning. First, we confirm the debuckling and roughening of the (110) surfaces by hydrogen adsorption at the atomic level. This was predicted by Ref. [3] from methods showing integral information without atomic resolution. We see both effects in images with atomic resolution: Hydrogen adsorption debuckles the surface while the roughening is in fact related to the formation of very specific defects derived from arsenic vacancies. Further, we link the structural changes to changes in electronic properties and confirm our STS results by tunnel current simulations. Second, the effects of hydrogen cleaning itself are shown in images with atomic resolution. Two effects are observed: The formation of native defects as well as the (re)creation of atomically flat surfaces. Again, electronic properties are evaluated from tunneling spectra and confirmed by tunnel current simulations. These findings lead to a comprehensive picture of the processes involved in the hydrogen cleaning procedure of III/V semiconductor surfaces.

The authors thank the Deutsche Forschungsgemeinschaft – Project number 390247238 - for financial support.

[1] Motohisa et al., Phys. E 23, 298 (2004)

[2] Webb et al., Nano Lett. 15, 4865-4875 (2015)

[3] M'Hamedi et al., Semicond Sci Technol 2, 418 (1987)

11:00am **PCSI-MoM2-31 Surface Work Function Engineering of Diamond-like Carbon Through Spatial Selective Gallium Implantation***, **Jiayun Liang,** Z. Al Balushi,* University of California at Berkeley

Bottom-up synthesis of materials with high spatial selectivity has long been a goal of nanotechnology. However, to obtain spatially selective nucleation and exact control over the size and shape of the domain during the synthesis, spatial modification of the surface work function landscape of substrate must be realized at the growth temperature. Herein, a spatially controllable surface work function landscape of diamond-like carbon (DLC) thin layer was achieved through spatially selective implantation of gallium into DLC using focused ion beam (FIB). Under various FIB conditions, two typical features with a size of 5 µm and 5 µm were obtained: "valley" with a step height of 3.5 nm, and "hill" with a step height of 4 nm. Gallium precipitated after one-hour-long in-situ annealing process at 500°C or 300°C in a high-vacuum environment (10^{-9}torr). At 500°C, the surface work function of valley feature was 51 meV higher than that of the unimplanted region, while the surface work function of hill feature was 16.8 meV lower than that of the unimplanted region. However, as the annealing temperature dropped to 300°C, the surface work functions for hill and valley featuressurface were 51.8 meV and 88 meV lower than those of the unimplanted region, respectively. Both gallium precipitation and change of DLC properties contributed to the shift in surface work function. Therefore, a spatially controllable surface work function landscape can be realized by carefully tuning the annealing conditions and spatial arrangement of hill and valley features, facilitating the selective area growth of materials in various nanofabrication processes.

11:05am **PCSI-MoM2-32 Nanotrench Formation along Step Edges of Vicinal Si(111) Surfaces by Wet-chemical Treatments***, **Kenta Arima,** Z. Ma, T. Takeuchi, R. Hashimoto, R. Sun, K. Yamamura,* Osaka University, Japan

We aim at forming atomic-thick Si ribbons from a silicon-on-insulator (SOI) layer possessing a vicinal (111) surface by combining multiple wet-chemical treatments. Among the treatments, the most important one is to cut neighboring Si terraces along atomic step edges by metal-assisted chemical etching (MacEtch). To test this MacEtch performance, we have started experiments using a Si(111) bulk wafer. The Si surface has the miscut angle of 0.2°.

After a cut sample was wet cleaned, it was immersed in water in which the concentration of dissolved O_2 molecules was very low, or a ppb level. This process is referred to as the first LOW (Low dissolved-O_2 Water) treatment. We find that a Si(111) surface composed of flat terraces and biatomic steps was formed by this first LOW treatment. Then it was immersed in LOW containing Ag^+ ions at a concentration of 5 ppm, which is referred to as the second LOW treatment. It was demonstrated that Ag atoms were selectively reduced at the edges of atomic steps on Si(111) to form Ag nanowires, as reported by another group. Finally, the Si sample with Ag nanowires was immersed into a mixture of HF and H_2O_2. The resultant AFM image indicates that the self-assembled Ag nanowires after the second LOW treatment were replaced by almost continuous nanotrenches. This is probably because the Ag nanowires acted as a catalyst to enhance chemical etching of the Si surface underneath [1]. By applying this sequence for a thin SOI layer, we expect to form Si ribbons of which both a width and a thickness are controlled in a self-assembled manner.

[1] Z. Ma, S Masumoto, K. Kawai, K. Yamamura, and K. Arima, *Langmuir*, **38**, 3748 (2022).

11:10am **PCSI-MoM2-33 III-V Materials Grown Directly on V-groove Si for Solar Cells***, **Theresa Saenz,** J. Mangum, J. Boyer, A. Neumann, R. France, W. McMahon,* National Renewable Energy Laboratory*; J. Zimmerman,* Colorado School of Mines*; E. Warren,* National Renewable Energy Laboratory

III-V solar cells offer superior performance to other technologies, reaching light conversion efficiencies above 40% [1]. However, their high cost has limited their use to space applications, with the GaAs or Ge substrate contributing a large portion of the overall cost [2]. The direct growth of III-Vs on Si is a compelling strategy to combine the high performance of III-V solar cells with the low cost of Si substrates. Nanopatterned V-groove Si offers both additional cost savings through its compatibility with low-cost wafer polishing and an ideal crystallographic surface for preventing the formation of antiphase domains that typically plague III-V on Si growth. In this work, we demonstrate the growth of low-dislocation-density GaAs on GaP grown via metalorganic vapor phase epitaxy (MOVPE) on V-groove Si substrates.

Fig. 1: a) SEM cross-sectional image of coalesced GaP on V-groove Si. b) AFM of the coalesced GaP with a R_q of 0.2 nm. c) ECCI image of GaAs on GaP on V-groove Si after TCA and DFLs showing a TDD of 3´10^6 cm^{-2}.

We studied a number of MOVPE nucleation conditions for GaP on V-groove Si and found that a high V/III ratio and growth temperature produces uniform nucleation at the bottom of the grooves that later coalescences into a thin film as shown by cross-sectional scanning electron microscopy (SEM, Fig. 3a) [3], with the exact geometry of the nanopatterns also playing an important role in coalescence. The coalesced GaP was very smooth, with a RMS roughness (R_q) of 0.2 nm measured by atomic force microscopy (AFM, Fig. 3b). However, with a threading dislocation density (TDD) of 5´10^7 cm^{-2} as measured by electron channeling contrast imaging (ECCI, Fig. 3c), the defects in this GaP on Si template would be limiting for solar cells applications. To decrease the TDD, we grew GaAs on the GaP/Si templates and employed thermal cycle annealing combined with a dislocation filter like the one described in Ref. 4. This resulted in relaxed GaAs with a TDD of 3´10^6 cm^{-2} as measured by ECCI, achieving a low TDD in a material with a

bandgap suitable for solar cells. We will present solar cell results and discuss the materials science consideration involved in achieving smooth and high-quality III-V growth on V-groove Si.

[1] M. A. Green, et al., Prog. Photovolt. **29**, 657-667 (2021).

[2] J. S. Ward et al., Prog. Photovolt. **24**, 1284-1292 (2016).

[3] T.E. Saenz et al., Crys. Growth Des. **20**, 6745-6751 (2020).

[4] C. Shang et al., Phys. Stat. Solidi A **218**, 2000402 (2021).

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11:15am **PCSI-MoM2-34 Improved Passivation Performance of Atomic-layer-deposited (ALD)-MoO_X Film by Introducing an Al_2O_3 Interlayer**, ***Hyo Sik Chang,*** Chungnam National University, Republic of Korea

The carrier-selective contact solar cell structure allows transition metal oxides to bend the band gap to stabilize energy, and adjusts the energy band to induce barrier tunneling such that holes and electrons can move efficiently to both electrodes, thereby reducing recombination loss and increasing efficiency. Conventional hole selection candidates, such as WO_X, VO_X, and MoO_X, have been investigated as hole-selective contacts (HSC) [1]. In this study, we introduce a low-temperature ALD-Al_2O_3 interlayer for continuous processing with the ALD-MoOx film. Therefore, based on the HSC structure using ALD-MoOx, we conducted a study on the change in passivation performance by controlling the ALD-MoO_X interface state by introducing ultra-thin ALD-Al_2O_3 grown at a low temperature of 170 °C, which is the same as the deposition temperature of ALD MoOx.The deposition rate of the ALD-MoO_X thin film using 250 g/Nm^3 ozone was approximately 0.036 nm/cycle. MoO_X deposition was performed at 150, 250, and 350 cycles for proper thickness selection of the carrier selective contact. The best passivation performance of the MoO_x thin film at 250-ALD cycle exhibits a carrier lifetime of 22 *us* and an implied *iVoc* of 568 *mV*, as shown in Fig. 1. Although the best values of the MoOx thin film are shown in the 250-ALD cycle, the passivation characteristics are relatively low. This phenomenon can be explained by the fact that thin SiO_X generated between MoO_X and Si substrates causes defects. the Al_2O_3 interlayer helps to reduce interface defects because Al_2O_3 layers reduce Si^{1+} and Si^{3+} sub-oxide states and changes to Si^{4+} to form network components that mimic SiO_2. This induces stabilization of the interface and the work function of the MoOx was found to ~7.0 eV. The composition of the MoO_3 thin film close to that of Mo^{6+} was confirmed.

[1] T. Zhang, C.-Y, Lee, Y. Wan, S. Lim, B. Hoex, , J. Appl. Phys. 124 (2018).

11:20am **PCSI-MoM2-35 UPGRADED: Determining the Arrangement of sub-Surface Dopants in a Silicon Quantum Device Platform**, ***Håkon Røst,*** Norwegian University of Science and Technology (NTNU), Norway*; E. Tosi,* Instituto de Ciencia de Materiales de Madrid, Spain*; F. Strand, A. Åsland,* Norwegian University of Science and Technology (NTNU), Norway*; P. Lacovig, S. Lizzit,* Elettra-Sincrotrone Trieste, Italy*; J. Wells,* University of Oslo, Norway

Recently, efforts to realize a silicon-based, CMOS-compatible quantum computer have been intensifying. Central to its development are so-called Si:P δ-layers: i.e., ultra-sharp layers of phosphorus atoms placed beneath the silicon surface [1]. Until recently, one key property has remained elusive: the arrangement of the P dopants within the δ-layer. The answer to this question is of crucial importance, as the dopant arrangement will directly impact the energy separation (i.e., valley-splitting) of the supported quantum well states [2].

In this talk, we will demonstrate how the local neighborhood around encapsulated dopants in a bulk semiconductor can be directly probed using X-ray photoelectron diffraction (XPD). By utilizing subtle core level energy shifts that are concomitant with the coordination of a dopant, chemically specific diffractive images can be formed [3]. Through comparison with XPD simulations that are derived from models of the local atomic environment around the dopants, the true dopant atom placement can be ascertained. Typically, XPD is only used as a probe of surface structure [4]. We demonstrate here that – under the right conditions, it also can be used to determine the local arrangement of sub-surface atoms. Therefore, XPD is well suited for solving the long-standing mystery of the Si:P δ-layer structure.

References:

[1] F. A. Zwanenburg *et al*., Rev. Mod. Phys. **85**, 961 (2013).

[2] D. J. Carter *et al*., Nanotechnology **22**, 065701 (2011).

[3] D. Woodruff, Surf. Sci. Rep. **62**, 1 (2007).

[4] A. J. U. Holt *et al*., 2D Mater. **8**, 035050 (2021).

11:40am **PCSI-MoM2-39 Cross-sectional Scanning Tunneling Microscopy Study of 6.1 Å Family Semiconductors for ULTRARAM™ Memory**, ***Aurelia Trevisan,*** Eindhoven University of Technology, The Netherlands*; P. Hodgson,* Lancaster University , UK*; D. Lane,* University of Adelaide, Australia*; M. Hayne,* Lancaster University, UK*; P. Koenraad,* Eindhoven University of Technology, The Netherlands

The peculiar band alignments of the 6.1 Å semiconductor family (InAs, GaSb and AlSb) have been exploited for the development of a new non-volatile memory technology, ULTRA**RAM**™[1]. The basis of the nonvolatility of ULTRA**RAM**™ is the large InAs/AlSb conduction band offset (2.1 eV). Multiple ultrathin InAs/AlSb heterojunctions form a triple-barrier resonant tunnelling (TBRT) structure between the channel and the floating gate (FG) [2]. Electrons are allowed to move across the TBRT layers when a low voltage is applied (~ 2.5 V), while when no bias is applied, electrons cannot be transferred in or out the FG [1]. ULTRA**RAM**™is presently grown by molecular beam epitaxy. However, for commercial production, the growth would be ideally transferred to MOCVD as it is more scalable. We performed room temperature and low temperature cross-sectional scanning tunneling microscopy (X-STM) measurements on a ULTRA**RAM**™sample grown on a GaAs n-doped wafer. With X-STM, the various layers of ULTRA**RAM**™ were investigated at the atomic scale. The main goal of the experiment was to probe the quality of the layers and their interfaces, in terms of thickness uniformity and sharpness, in particular the TBRT. In the investigated sample, the TBRT is positioned between an InGaAs layer (readout channel) and an InAs layer (FG). We studied the morphology of the TBRT, the quality of the InAs/AlSb layers and the uniformity in their composition. We observed the formation of slip planes starting from the interface between the InGaAs layer and the GaSb layer below it, most probably due to the lattice mismatch of the grown layers. The slip planes either end at the top most layer of the sample (FG) or at the interface between the InGaAs channel layer and the AlSb barrier B1. The latter typically give rise to small, down-triangle-shaped AlSb accumulation regions below B1 of the TBRT (Quantum Pits, QPs). However, we also observed the formation of AlSb QPs in the absence of an identified slip plane. Due to presence of the QPs the InGaAs/AlSb interface is not sharp and the thickness of B1 is uneven. Interestingly, the subsequent InAs and AlSb layers in the TBRT are typically characterized by sharper interfaces and more uniform thickness. We investigated possible mechanisms for the formation of the QPs and a possible relation with the presence of the slip planes.

[1] P. D. Hodgson, D. Lane, P. J. Carrington, E. Delli, R. Beanland, and M. Hayne, Adv. Electron. Mater., 2101103 (2022)

[2] D. Lane, M. Hayne, J. Phys. D: Appl. Phys. **54**, 355104 (2021)

11:45am **PCSI-MoM2-40 Surface Reaction and Plasma Induced Damage by Atomic Layer Etching Process**, ***Sung Gyu Pyo,*** Chung-Ang University, Republic of Korea

As the semiconductor integrated process enters the region below 10 nm, the removal of contaminants on the silicon wafer surface is crucial for high-integration device products and has a great influence on the yield, quality, and reliability of these products. Therefore, a cleaning method with high efficiency and high selectivity is required.

Correspondingly, the NOR (native oxide removal) dry cleaning method, which removes the native oxide films by using indirect plasma with hot H_2 or H_2/NF_3 gases, has attracted attention as a next-generation cleaning process because it can etch various thin-films with profile control. According to Toshio Hayashi et al. the mechanism for the dry cleaning process using hot H_2 gas and down flow NF_s gas, which are not decomposed at the plasma source, is that fluorine, which has high electronegativity, is adsorbed well on the surface of the silicon wafer and reacts with hydrogen gas; it then generates NH_4-F-NH_4 because of Coulomb interaction. Therefore, $(NH_4)_2SiF_6$ is formed on the silicon substrate and vaporized at above 100 °C.

Dry cleaning can control selectivity of the contaminants and roughness of the wafer surface, depending on gas flow, temperature, pressure, plasma power, and pressure distribution. However, controlling various process parameters is very difficult; It is necessary to understand the mechanism of gas reactions based on the plasma used for controlling etch rate and selective thin-film uniformity.

In this study, we investigated the method of surface planarization as well as removal of contaminants during dry cleaning using down flow H_2 and NH_3 gas. According to the gas flow, dry cleaning of oxide, nitride, and p-doped

wafers was performed. On analyzing the quality of each film, we propose an analysis method for controlling etch rate to selective thin-films and contaminants in a trench region below 10 nm.

In this experiment, the characteristics of each thin-film were analyzed by Raman spectroscopy, which can quantify and provide qualitative analysis of selective parts through beam focusing. When the characteristics of p-doped thin-films are analyzed by selective removal of oxide and nitride films, which are deposited on p-doped silicon in trenches with a width of 10 nm or less, we can use Raman spectroscopy to determine the appropriate etch rate and time.

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