Challenges in SiO_2/SiC Interface Engineering for SiC Power MOSFETs

T. Hosoi,[1,2] T. Shimura,[2] H. Watanabe[2]

[1] *School of Engineering, Kwansei Gakuin University, Sanda, Hyogo, Japan*

[2] *Graduate School of Engineering, Osaka University, Suita, Osaka, Japan*

High on-resistance due to low channel mobility and threshold voltage instability due to charge trapping are major concerns of SiC-based power MOSFET, and both issues are deeply correlated with poor SiO_2/SiC interface property grown by thermal oxidation. One of the main causes of this severe interface degradation is residual carbon impurity remained near SiO_2/SiC interface. Although the most common technique to improve SiO_2/SiC interface quality is N incorporation into SiO_2/SiC interface by post-oxidation annealing in NO (NO-POA), the effect on mobility improvement is limited [1] and enhanced hole trapping is pointed out [2]. In this talk, we review the scheme of thermal oxidation and control of N atom profile to improve performance and reliability of SiC MOSFETs based on our recent results.

We demonstrated ultrahigh-temperature oxidation at low oxygen partial pressure to enhance C ejection from SiO_2/SiC interface during thermal oxidation [3]. Passive/active oxidation boundary for 4H-SiC(0001) surface was found to be at around 1600°C under 0.3% O_2/Ar ambient. As shown in Fig. 1(a), nearly ideal C-V curve can be obtained by ultrahigh-temperature oxidation, while large hysteresis and positive flatband voltage shift were observed for conventional oxidation. The field-effect mobility increased from 3 to about 10 cm^2/Vs by performing ultrahigh-temperature oxidation (Fig. 1(b)). The reduction in C-related defects was confirmed by electron-spin-resonance (ESR) spectroscopy [4]. We also found that SiC can be oxidized to form SiO_2 under CO_2 ambient at ultrahigh temperatures [5]. Furthermore, a combination of NO-POA and subsequent CO_2 annealing at moderate temperature is effective in obtaining high-channel mobility and stable threshold voltage thanks to the selective removal of N atoms on SiO_2 side at SiO_2/SiC interface and compensation of oxygen vacancies [6].

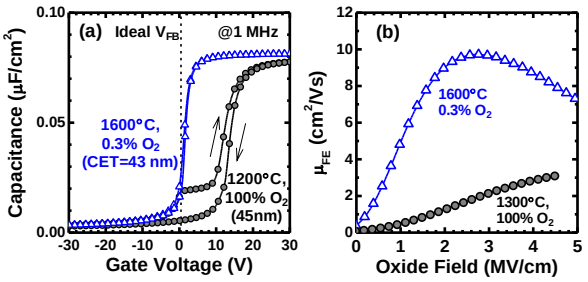

Figure 1 (a) C-V characteristics of MOS capacitors and (b) field-effect mobilities of MOSFETs with conventional thermal oxidation (1200-1300°C) and ultrahigh-temperature oxidation (1600°C) under low O_2 partial pressure [3].

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+ Author for correspondence: hosoi.takuji@kwansei.ac.jp